

Intel Sky Lake Platform

SLK-S CPU / SLK PCH-H

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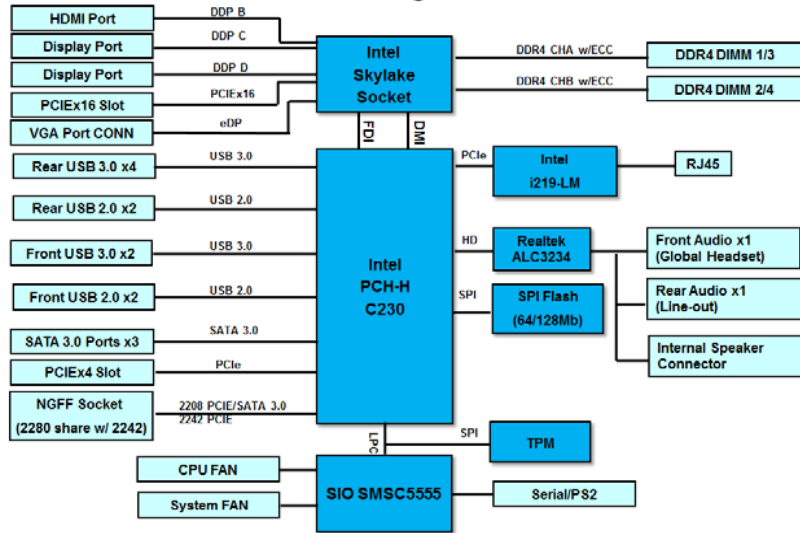
DO NOT DISTRIBUTE

Marking	Description
I	Installed
NI	Not Installed
MP	Production Part ONLY
PROTO	Not For Production Part
CCL	Critical Components List

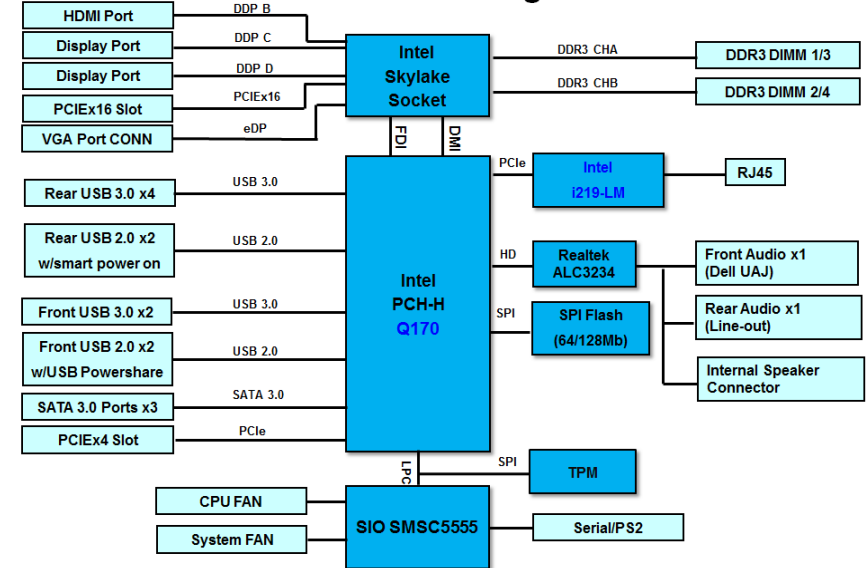
PCA P/N, Scorpion/Spitfire/Toledo	
SCH P/N, Scorpion/Spitfire/Toledo	
PCB P/N, Scorpion/Spitfire/Toledo	

	
INC.	
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Farallon SFF MB Block Diagram

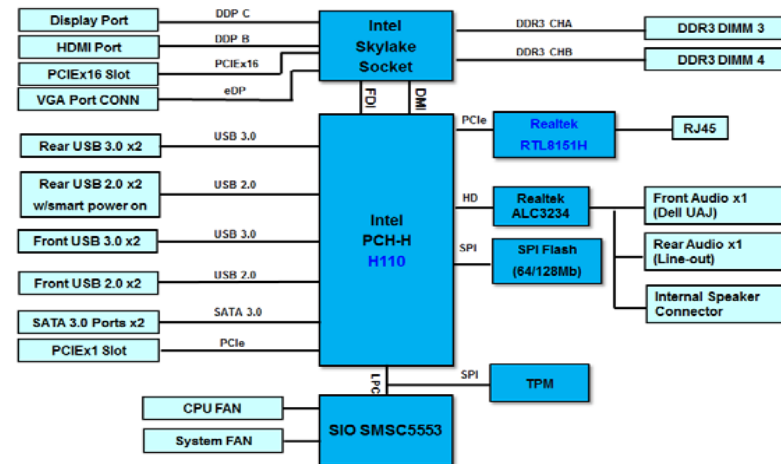


Swordfish SFF 9 MB Block Diagram

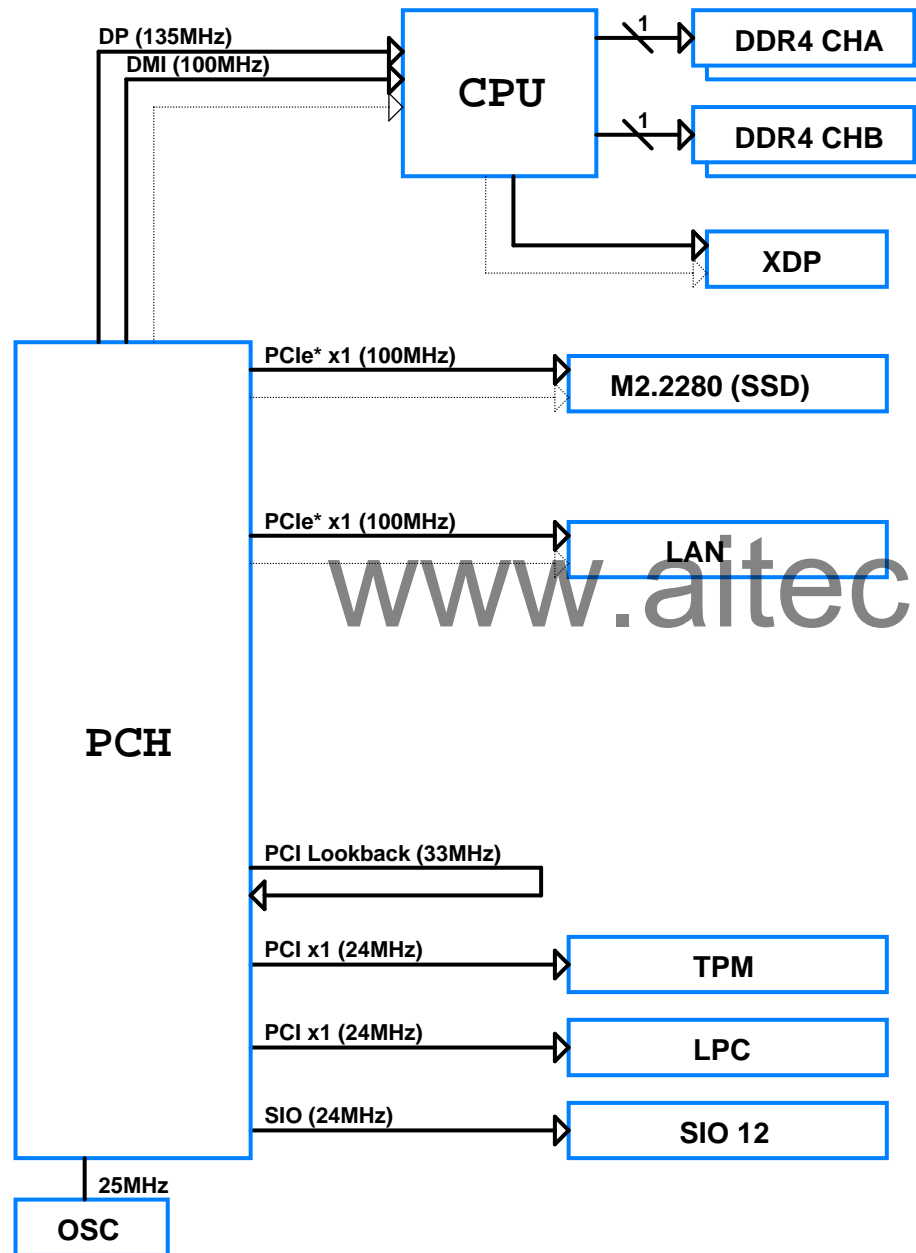


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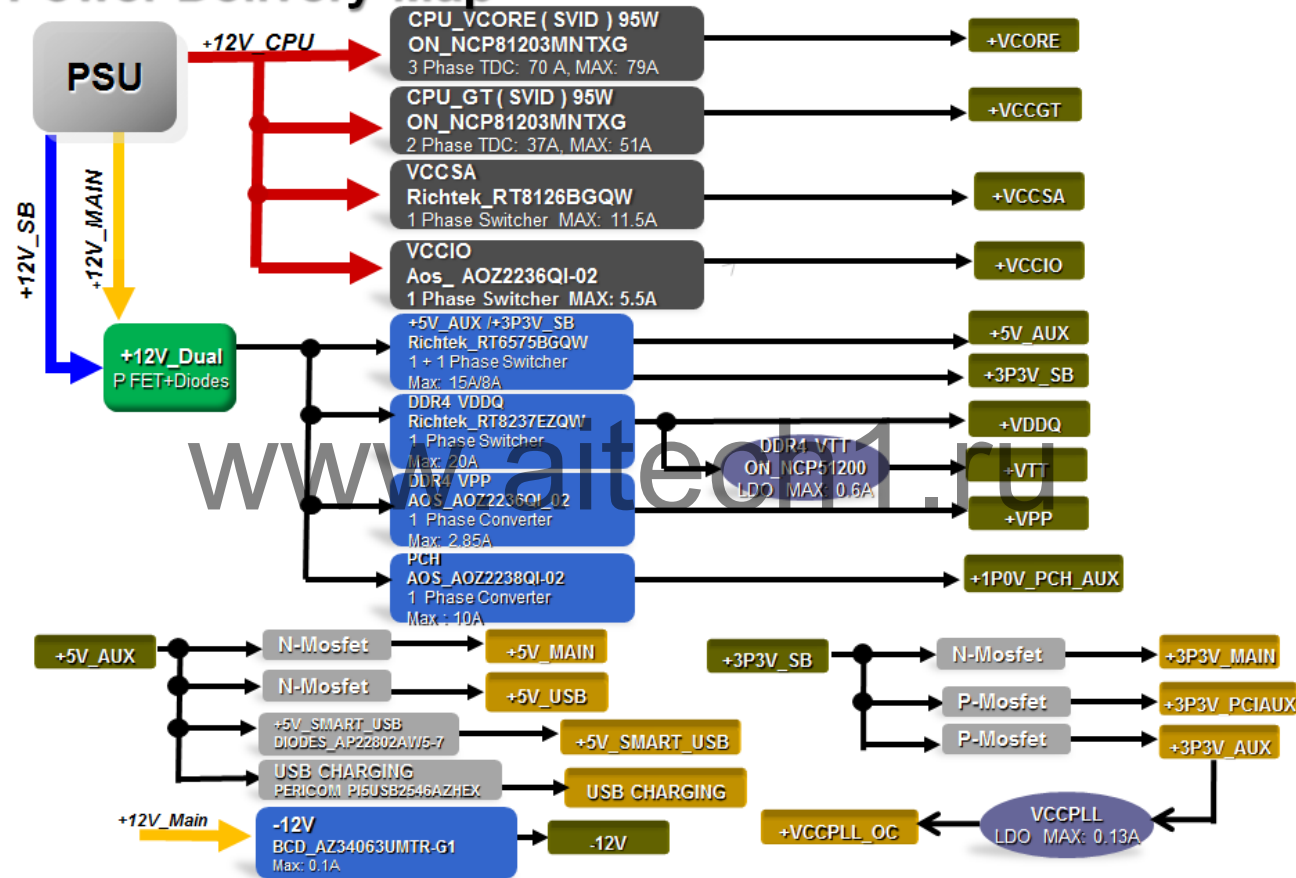
Swordfish SFF 3 MB Block Diagram



Clock Diagram




Power Delivery Map



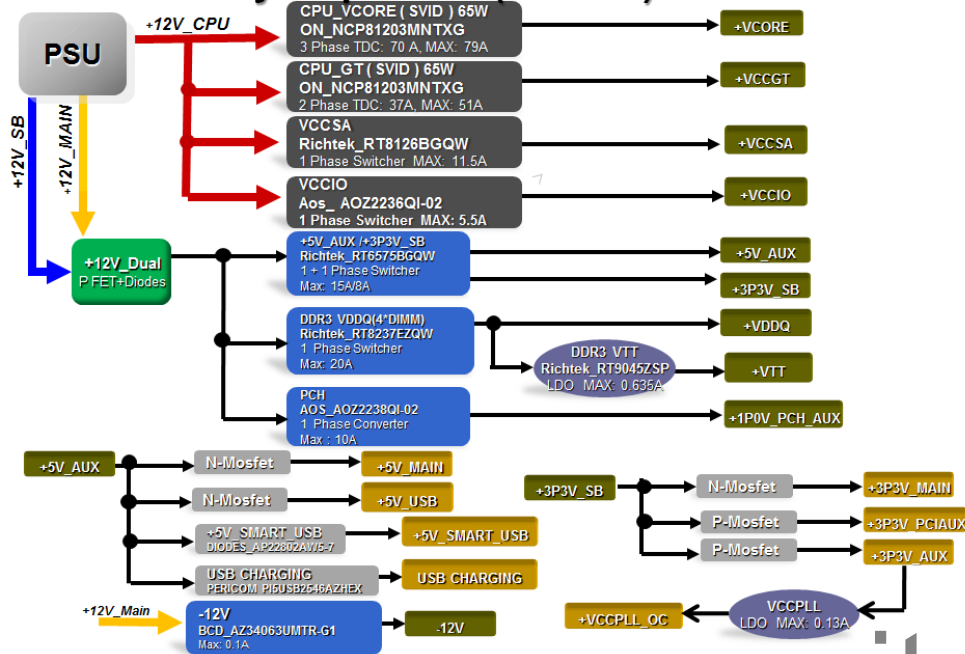
[illegible]

Signal	Usage	When Sampled	Comment
			<p>The signal has a weak internal pull-up.</p> <p>0 = Enable "Top-Block Swap" mode - PCH will invert A16 for cycles going to the upper two 64 KB blocks in the FWH or appropriate address lines (A16, A17, A18, A19 or A20) as selected in BIOS Boot-Block size software for SPT.</p> <p>1 = Disable "Top-Block Swap" mode.</p> <p>NOTES:</p> <ol style="list-style-type: none"> 1. The internal pull-up is disabled after PLTRST# deasserts. 2. Software will not be able to clear the Top-Block Swap bit until the system is rebooted. 3. This signal is in the Core well. 4. The status of this strap is readable using the Top-Block Swap bit (Chipset Config Registers: RCBA + Offset 3414h-Bit 0).
GPIO55	Top-Block Swap Override	Rising edge of PWOK	
DOPB_CTRLDATA	Port B Detected	Rising edge of PWOK	<p>This signal has a weak internal pull-down.</p> <p>0 = Port B is not detected. 1 = Port B is detected.</p> <p>NOTES:</p> <ol style="list-style-type: none"> 1. The internal pull-down is disabled after PLTRST# deasserts.
DOPC_CTRLDATA	Port C Detected	Rising edge of PWOK	<p>This signal has a weak internal pull-down.</p> <p>0 = Port C is not detected. 1 = Port C is detected.</p> <p>NOTES:</p> <ol style="list-style-type: none"> 1. The internal pull-down is disabled after PLTRST# deasserts.
DOPD_CTRLDATA	Port D Detected	Rising edge of PWOK	<p>This signal has a weak internal pull-down.</p> <p>0 = Port D is not detected. 1 = Port D is detected.</p> <p>NOTES:</p> <ol style="list-style-type: none"> 1. The internal pull-down is disabled after PLTRST# deasserts.

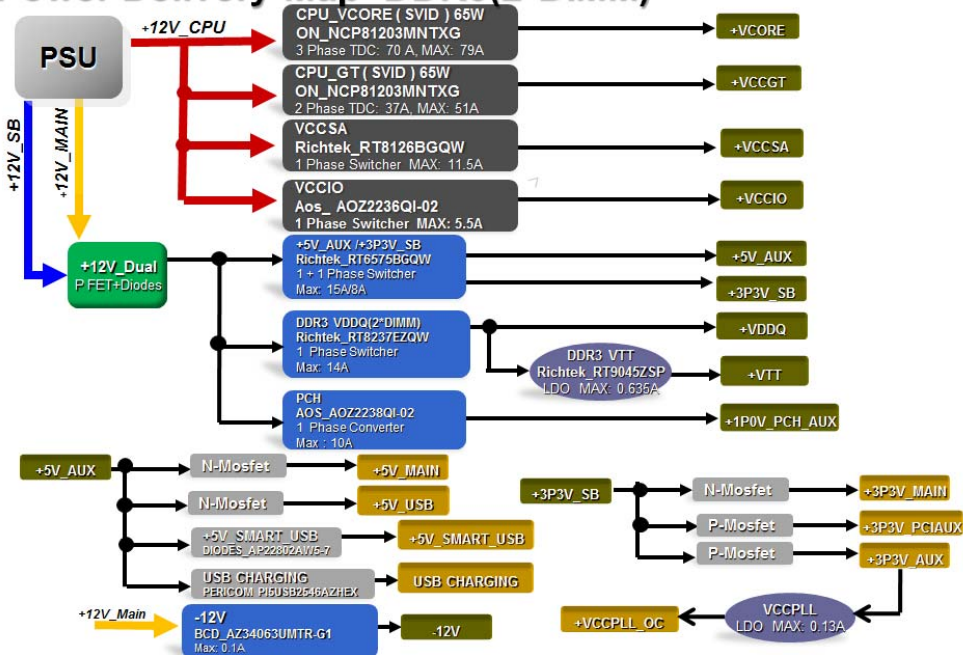
Signal	Usage	When Sampled	Comment
HDA_SDO	Flash Descriptor Security Override	Rising edge of PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Enable security measures defined in the Flash Descriptor</p> <p>1 = Disable Flash Descriptor Security (<i>override</i>). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.</p> <p>NOTES:</p> <ol style="list-style-type: none"> The weak internal pull-down is disabled after PLTRST# deasserts. Asserting the HDA_SDO high on the rising edge of PWROK will also halt Intel® Management Engine after chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug. This signal is in the Suspend well.
HDA_DOCK_EN# GPIO33	Reserved	Rising edge of PWROK	<p>This signal has a weak internal pull-down.</p> <p>NOTES:</p> <ol style="list-style-type: none"> The internal pull-down is disabled after PLTRST# deasserts. This signal should not be pulled high when strap is sampled. <p>This signal does not have an internal resistor; an external resistor is required.</p> <p>0 = DCPSU01, DCPSU02 and DCPSU03 are powered from an external power source (should be connected to an external VRM). External VRM powering option is for Mobile Only. Other systems should not pull the strap low.</p> <p>1 = Integrated VRMs enabled. DCPSU01, DCPSU02 and DCPSU03 can be left floating.</p> <p>NOTES:</p> <ol style="list-style-type: none"> This signal is always sampled. This signal is in the RTC well.
INTVRMEN	Integrated VRM Enable	Always	<p>This signal has a weak internal pull-up.</p> <p>0 = Disable PLL On-Die voltage regulator.</p> <p>1 = Enable PLL On-Die voltage regulator.</p> <p>NOTES:</p> <ol style="list-style-type: none"> The internal pull-up is disabled after RSMRST# deasserts. This signal is in the Suspend well.
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	Rising edge of RSMRST#	<p>This signal has a weak internal pull-up.</p> <p>0 = Disable PLL On-Die voltage regulator.</p> <p>1 = Enable PLL On-Die voltage regulator.</p> <p>NOTES:</p> <ol style="list-style-type: none"> The internal pull-up is disabled after RSMRST# deasserts. This signal is in the Suspend well.

			
Title			
STRAP and GPIO			
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Power Delivery Map DDR3(4*DIMM)



Power Delivery Map DDR3(2*DIMM)



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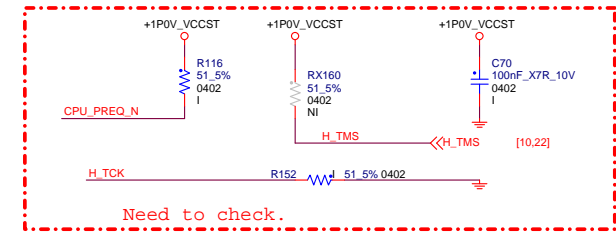
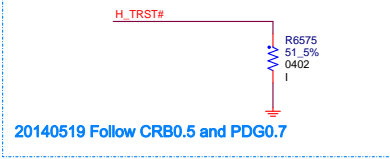


Title
Interrupt & PME

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20140520 Need check Debug port PDG



Intel MCP XDP Debug Connector

PREQ# and PRDY# MUST be routed in this order: Debug Port -> CPU -> PCH-H.
place R148, R149 close to CPU
20140520 Follow CRB0.5 and PDG0.7

CRB is dummy R148, R149
PDG is Pop R148, R149

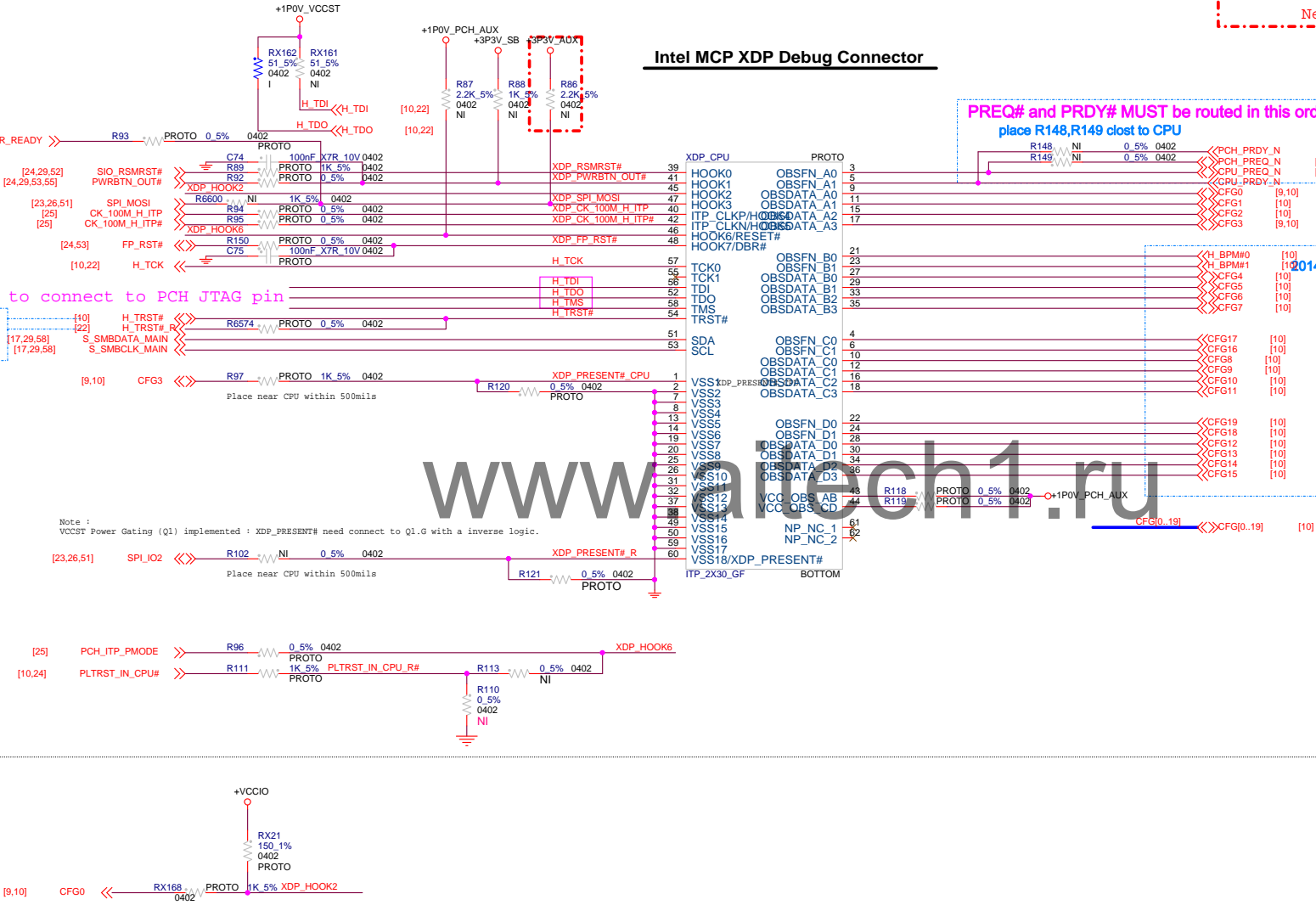
Need to connect to PCH JTAC pin

20140520 Follow CRB0.5 and PDG0.7

20140519 Follow CRB0.5 and PDG0.7

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Note :
VCCST Power Gating (Q1) implemented : XDP_PRESENT# need connect to Q1.G with a inverse logic.



APU - VID,CTRL, MSIC

+1P0V_VCCST +1P0V_VCCST +1P0V_VCCST

R7 56.2_1% 0402

R8 100_1% 0402

R9 90.9_1% 0402 NI

1P0V_VCCST ○ R51 NI1K_5%0402 H_CATERR#

1P0V_VCCST ○ R52 NI1K_5%0402 VR_HOT

20140516 CRB0.5 add RS
33 ohm , but PDG0.7 is 20
ohm , need check Intel

20140519 Need check with
Intel about RS value .
(CRB is 0 ohm , PDG0.7 is
500 ohm)

20140519 Change net name
to H_SKTOCC#

20140516 SKL-S EDS0.75:It should be connected to VCCIO with pull-up resistor of xx

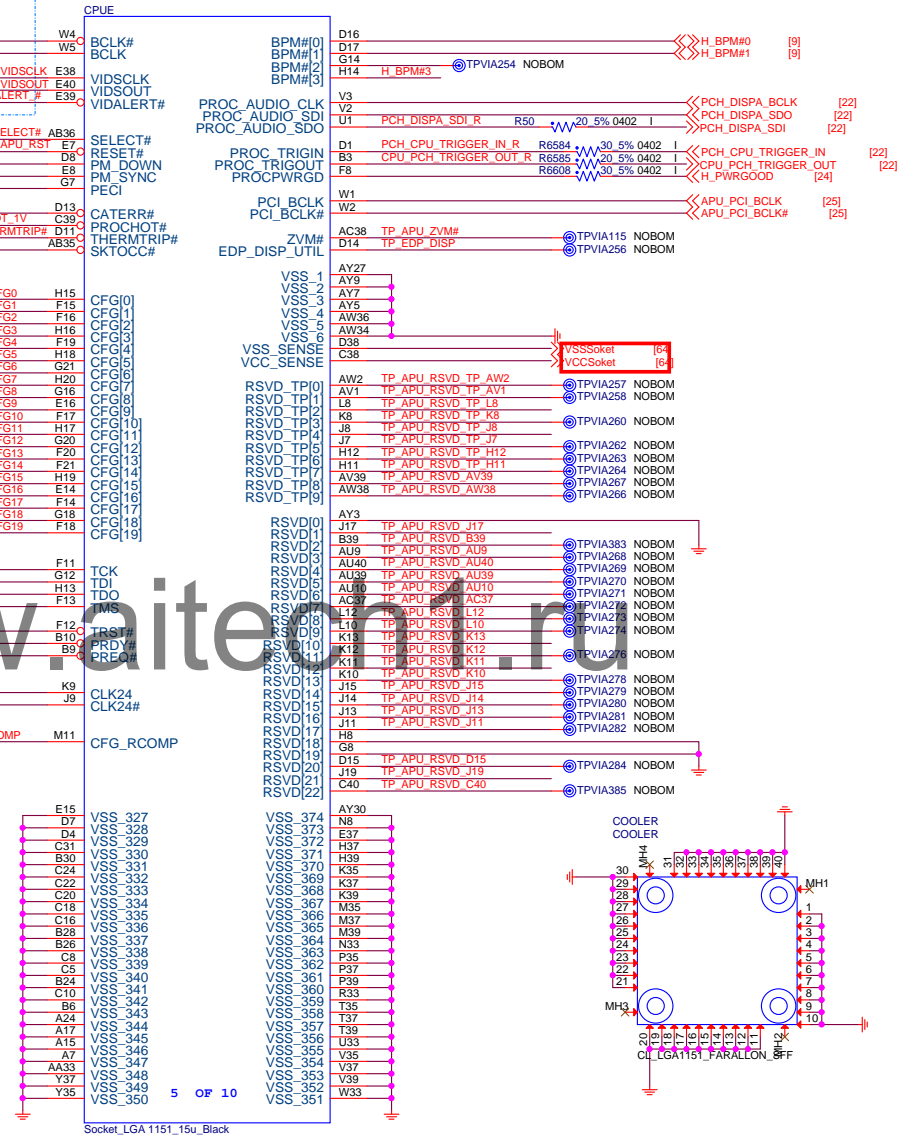
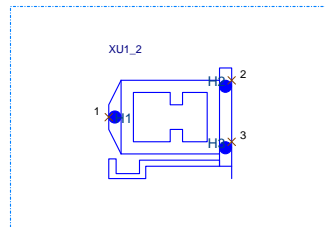
20140520 PU EDS0.75 "Stuff
R47 for Enable eDP ,unstuff
R38, R1 for PCIe X16

20140520 EDS0.75 CFG[19:8]:
Reserved configuration
lanes.

SKL S has adequate internal bias resistance on JTAG, PROC_PRDY# to keep the devices in an idel state without the external pull resistors.

PEI-E CONFIG TABLE		
CFG5	CFG6	PCI-E CONFIG
0	0	X8 X4 X4
0	1	RESERVED
1	0	X8 X8
1	1	X16

CFG	High	Low	Strap Description
0	NORMAL	STALL	EAR
1	NORMAL	PCHLESS	PCHLESS MODE
2	NORMAL	REVERSE	PEG LANE REVERSAL
3	ENABLE	DISABLE	PHYSICAL DEBUG ENABLE
4	DISABLE	ENABLE	eDP en/dis
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET_N	BIOS REQ	PEG DEFER TRAINING
8	DISABLE	ENABLE	CFG UNLOCK
9	PRESENT	NOT PRESENT	SVID NOT PRESENT
10	ACTIVE	DEACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DMI AC COUPLED
12	PMSYNC 2.0	LEGACY	PMSYNC LEGACY
13	SYNC	ASYNC	PMSYNC ASYNC MODE
14	RESERVED		
15	RESERVED		
ALL PINS HAVE INTERNAL PULL-UPS			




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Intel PCH XDP Debug Connector

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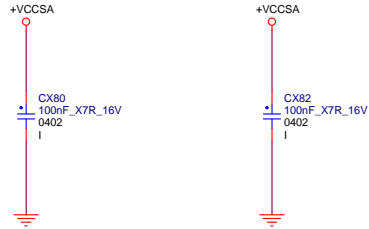
Project	
Spitfire	V
Scorpion	V
Toledo	V

 INC.	
Title	
CPU	
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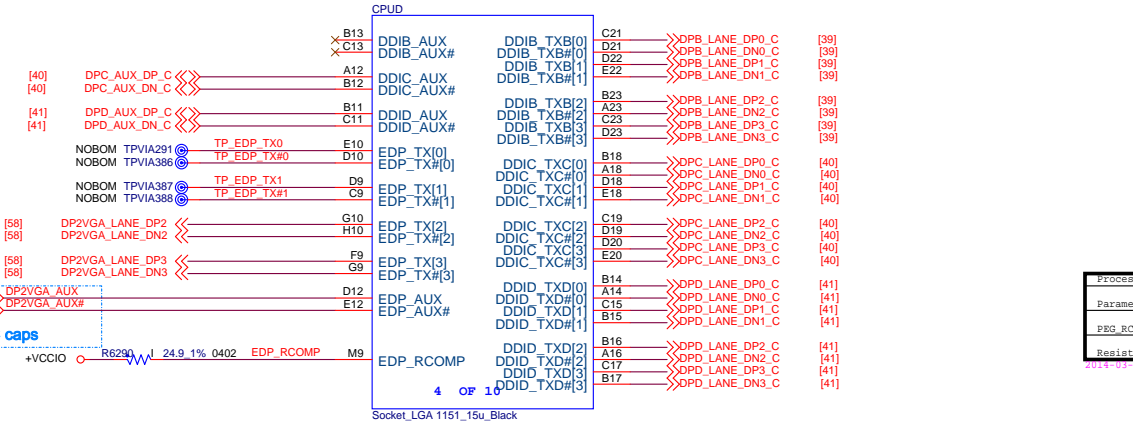
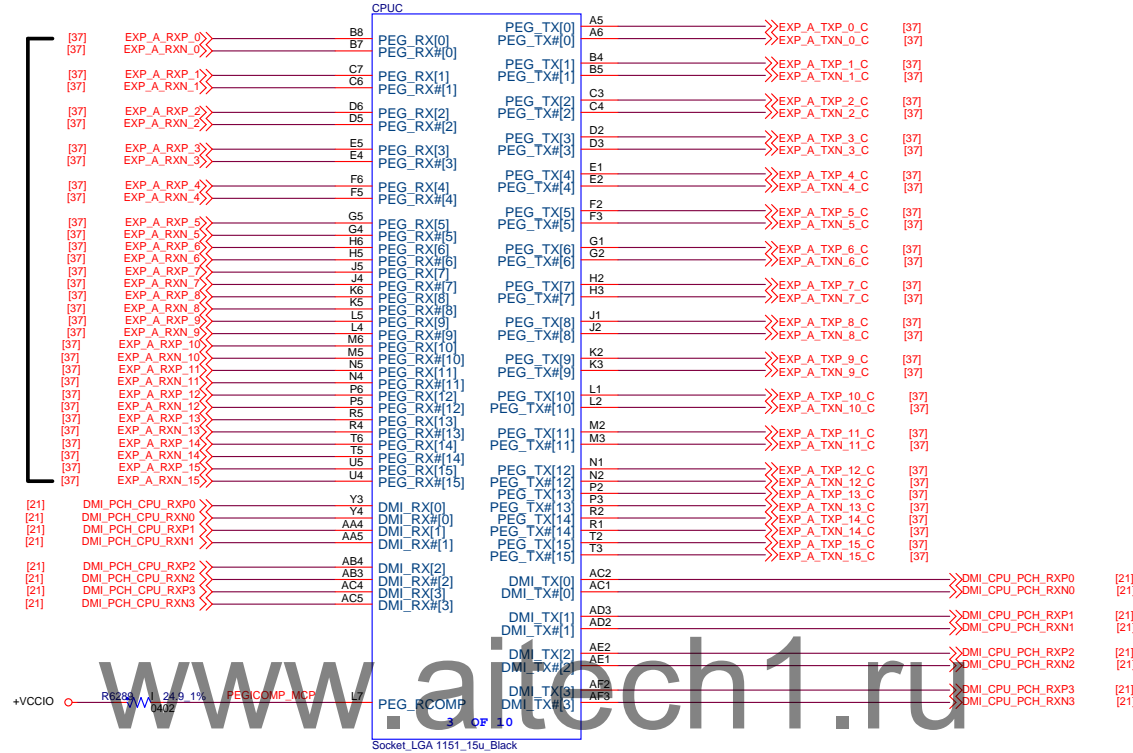
MCP - PCIE,DMI,FDI,DDI

PEG AC Cap Value		
Gen1/Gen2	75nf-265nf	
Gen3	180nf-365nf	

PEG x16 & DMI - Refer to PDG page45
 Breakout
 MS = 10/4/4/10
 DSL = 10/3/3.5/3/10
 Main
 12/3.5/4.5/3.5/12 (Group)
 15/3.5/4.5/3.5/15 (Other)



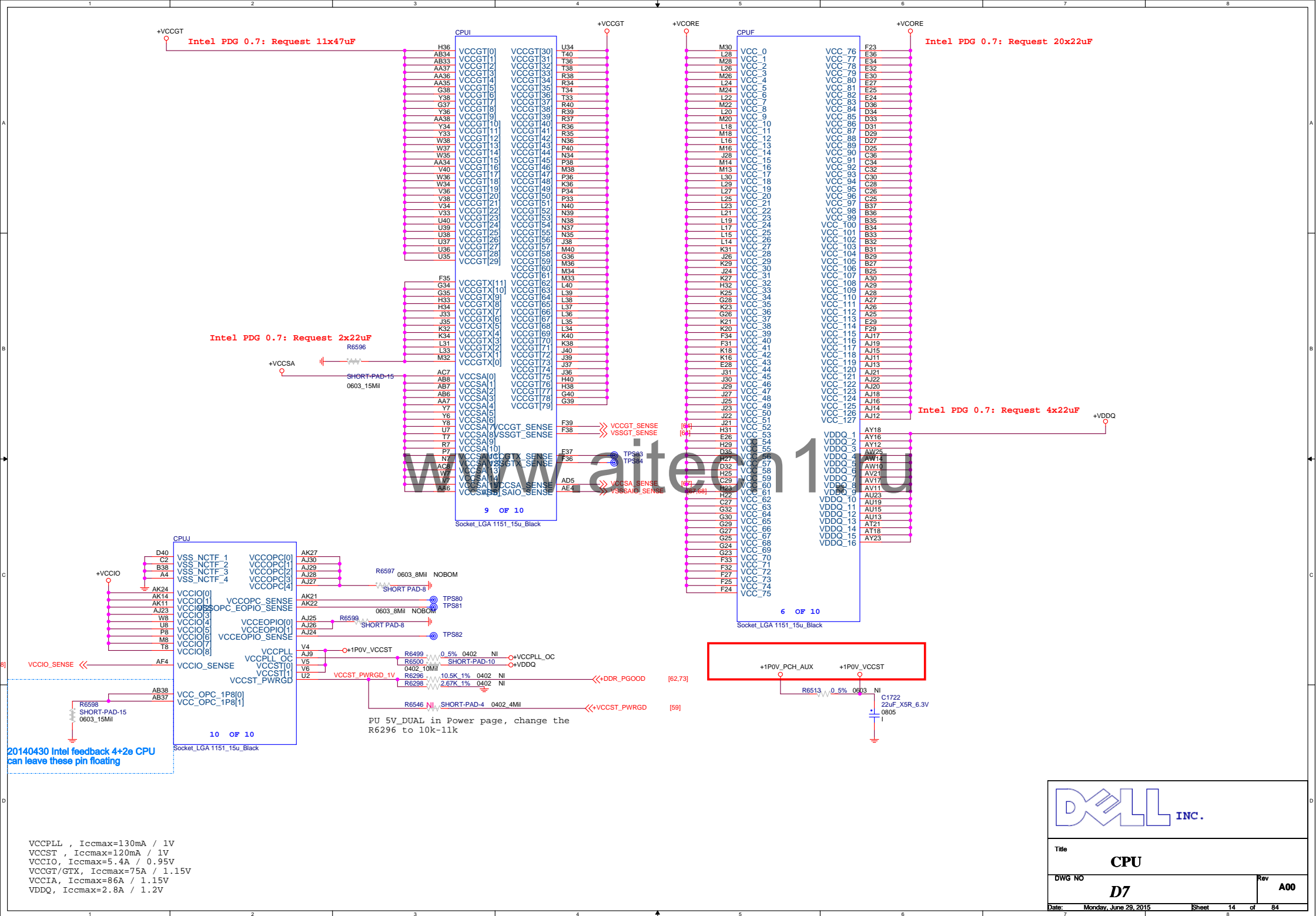
PEG_RCOMP:
 Trace Width = 12 mils
 Spacing = 15 mils
 Length = 400mils

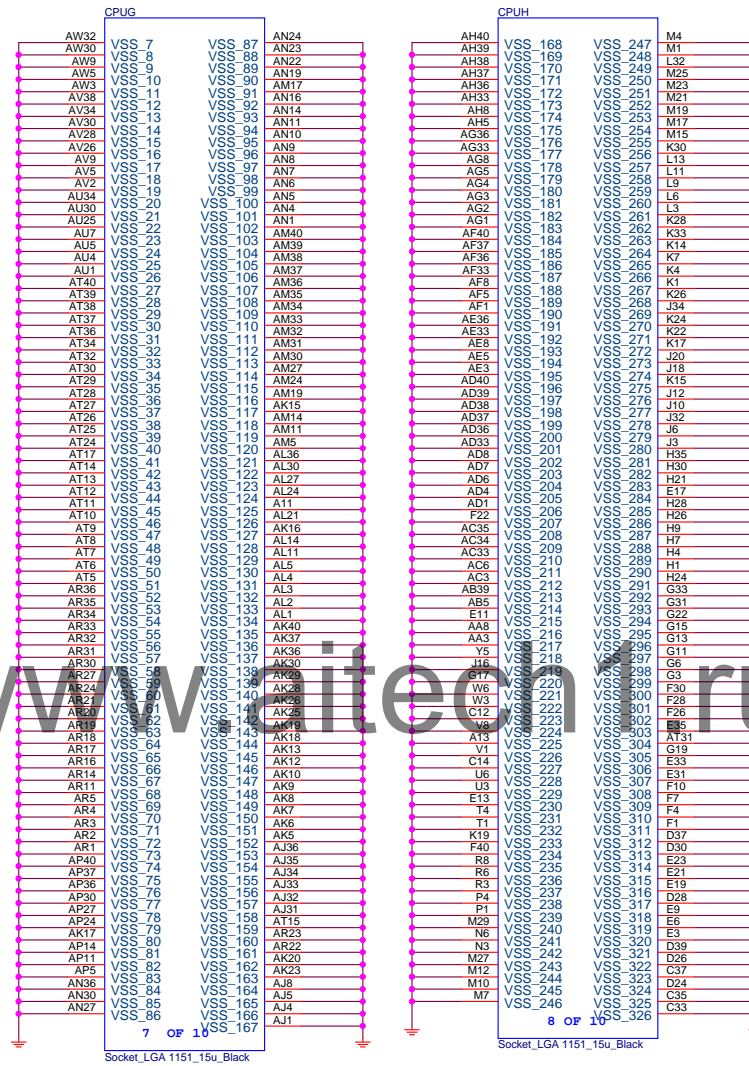


20140515 remove duplicated AC caps

Processor PCI Express® Compensation Signal Routing Guidelines					
Parameter	Units	Trace width	Trace spacing to other signals	Routing Length	Resistance
PEG_RCOMP	mils	12	15	400	24.9+-1%
Resistor	ohm				

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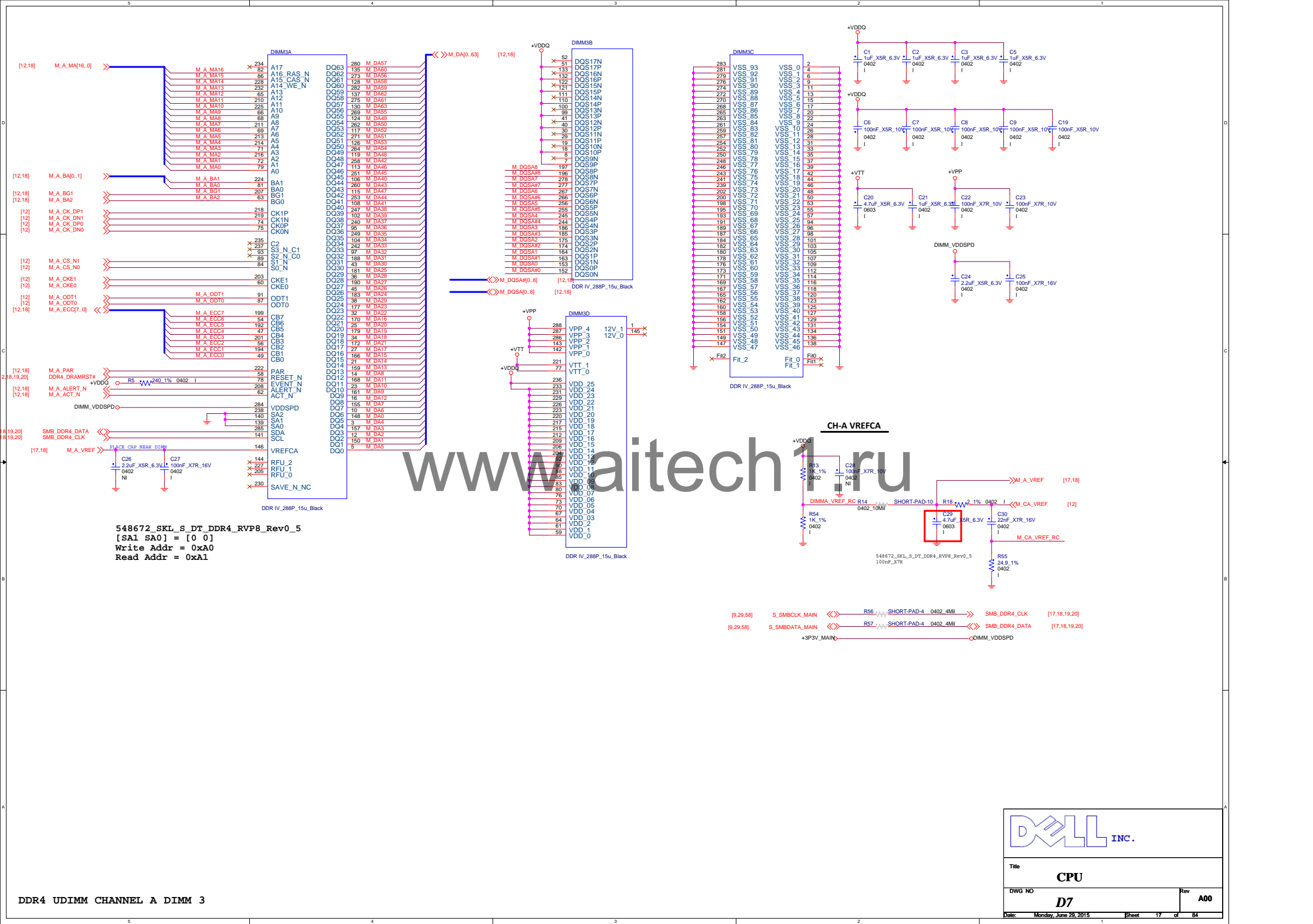


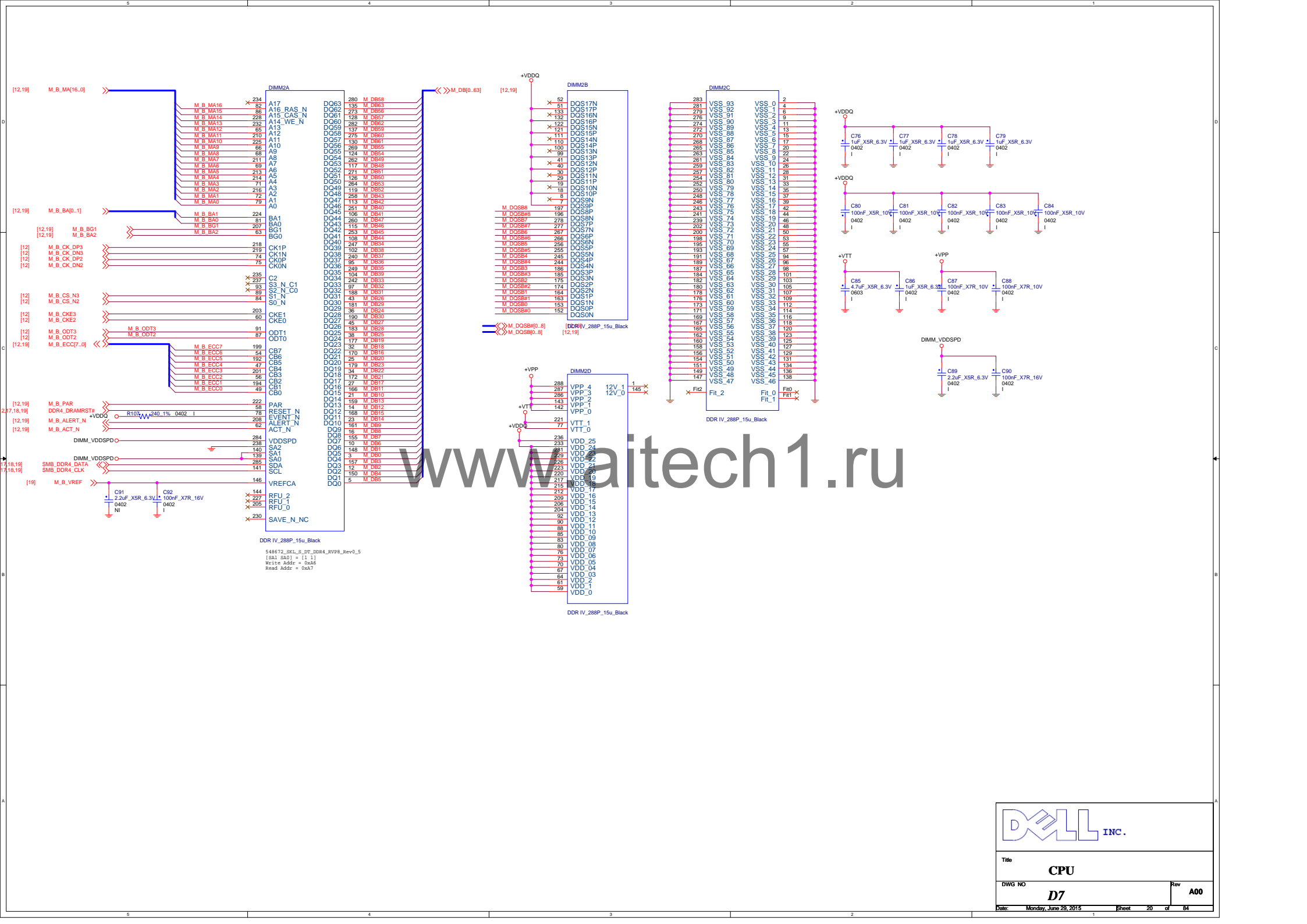
Intel PCH XDP Debug Connector

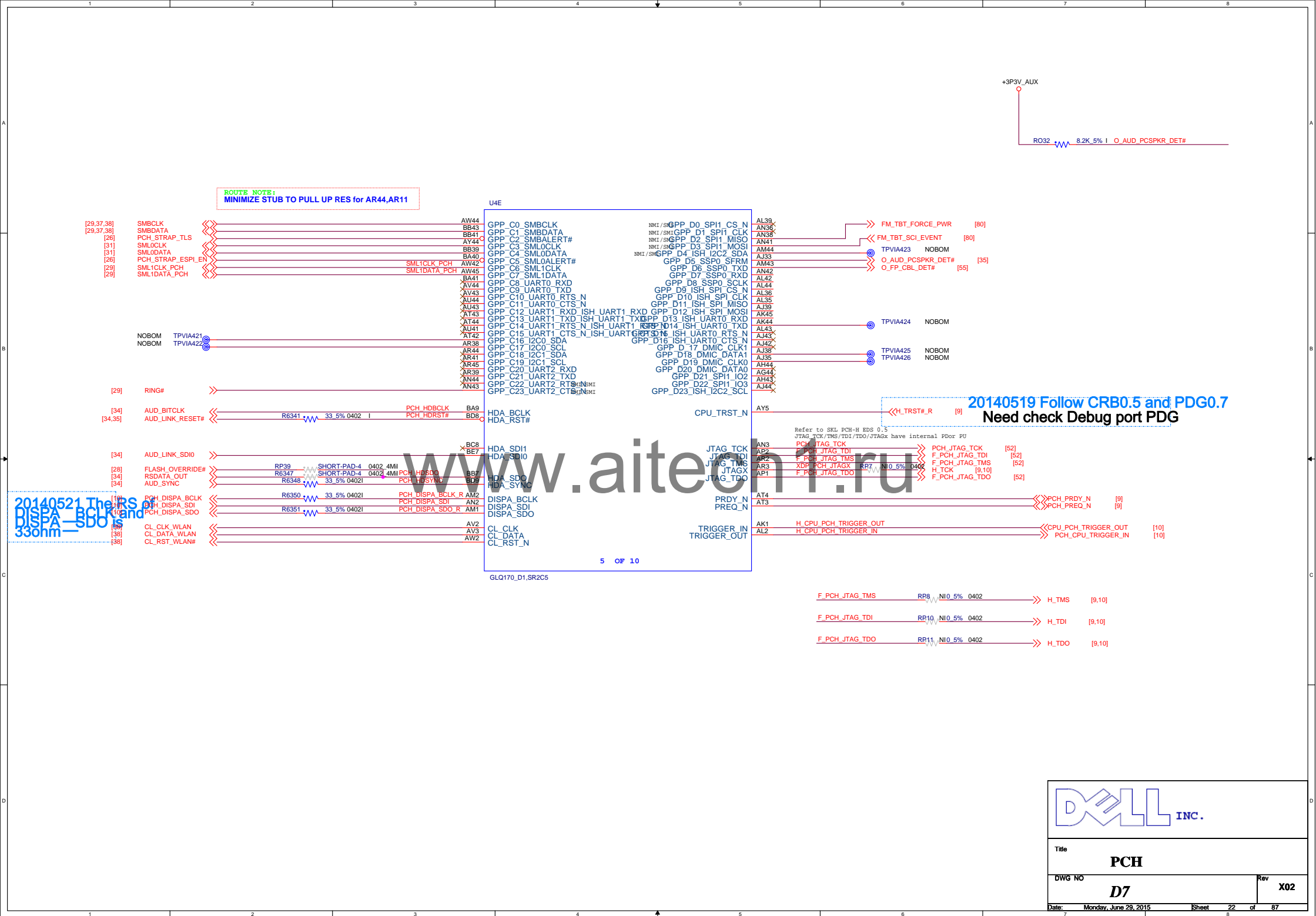
www.aitech1.ru

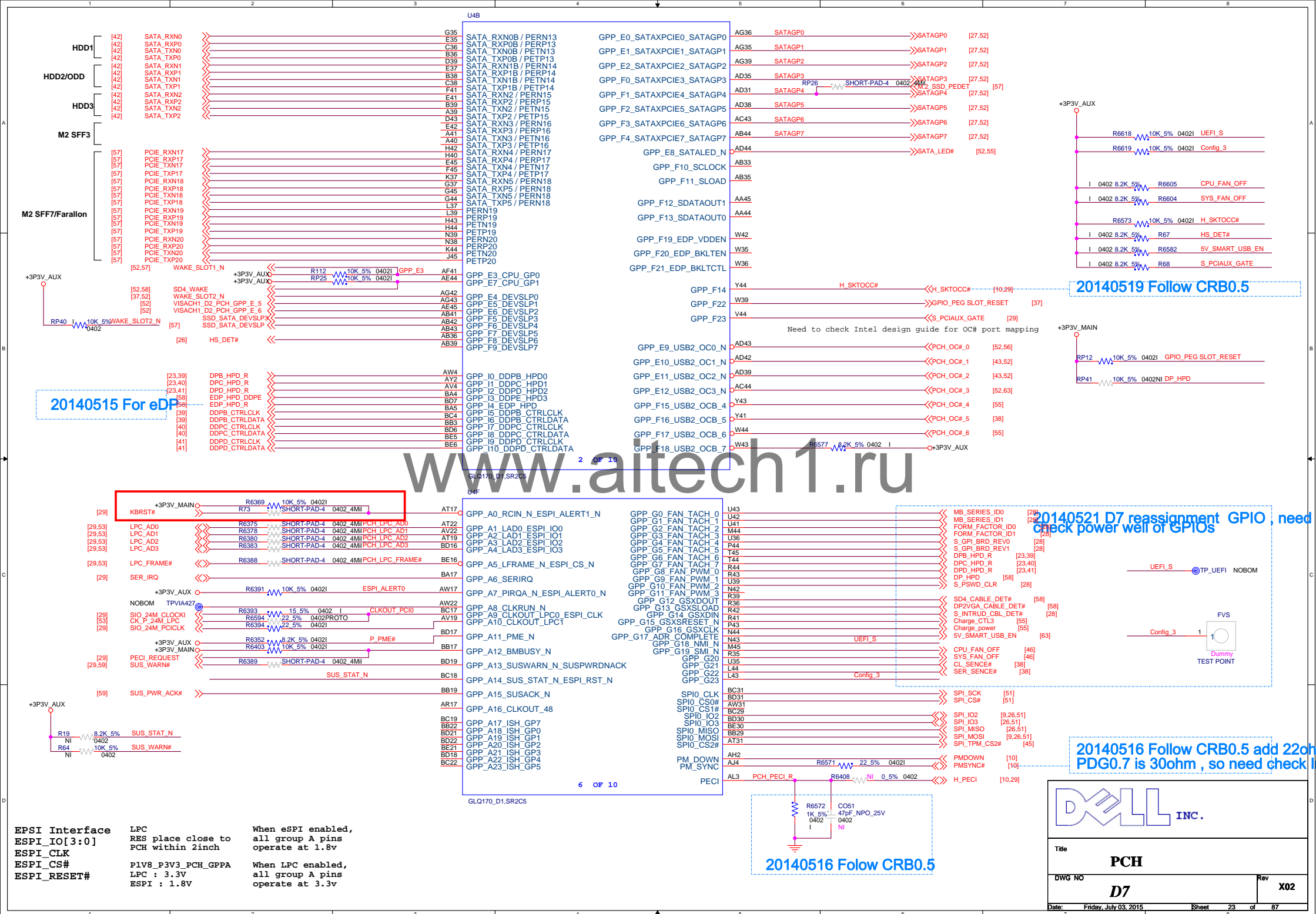
Project	
Spitfire	V
Scorpion	V
Toledo	V

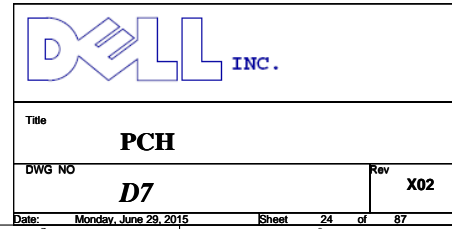
 INC.	
Title	
CPU	
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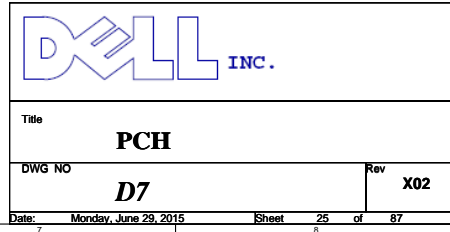




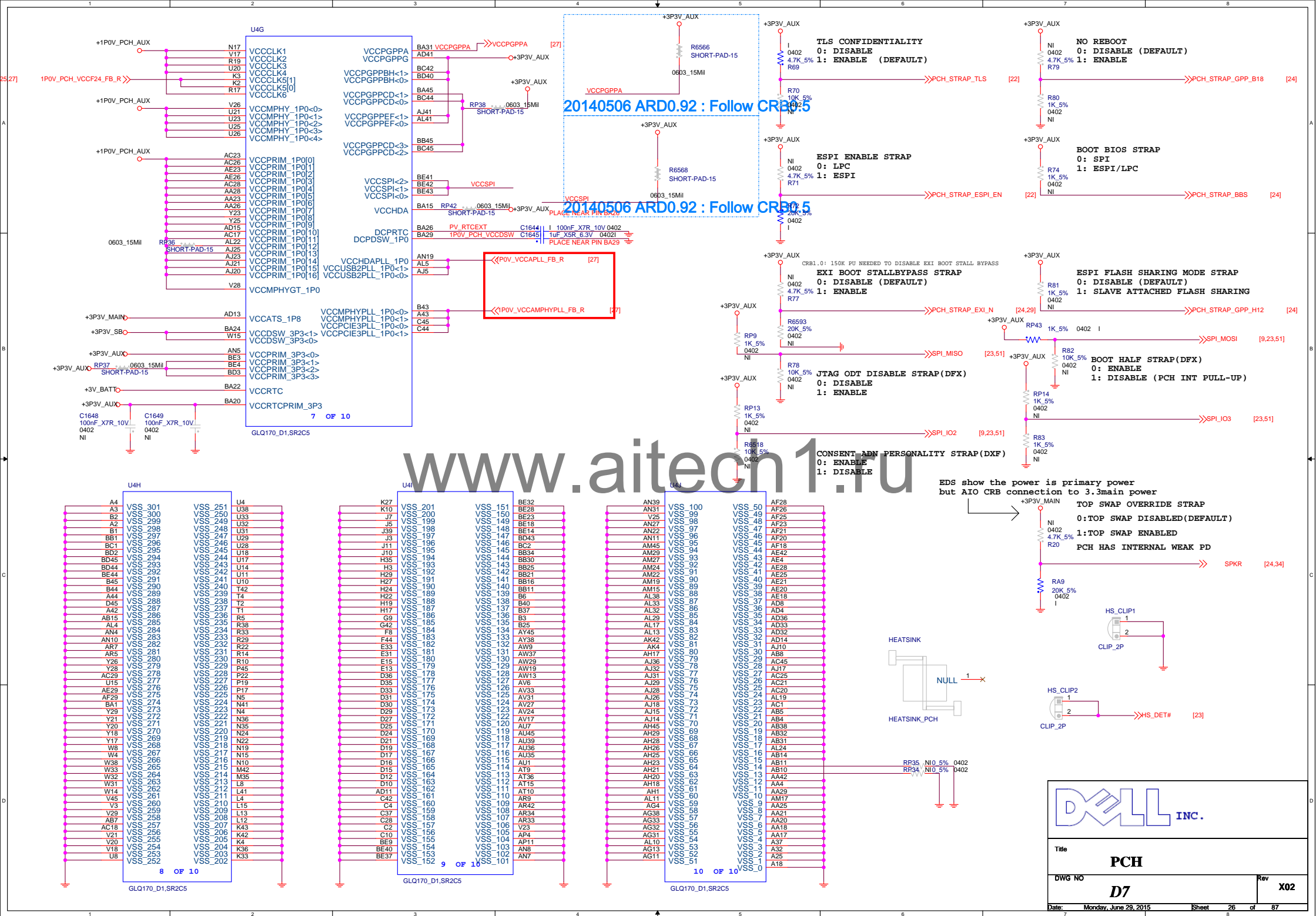




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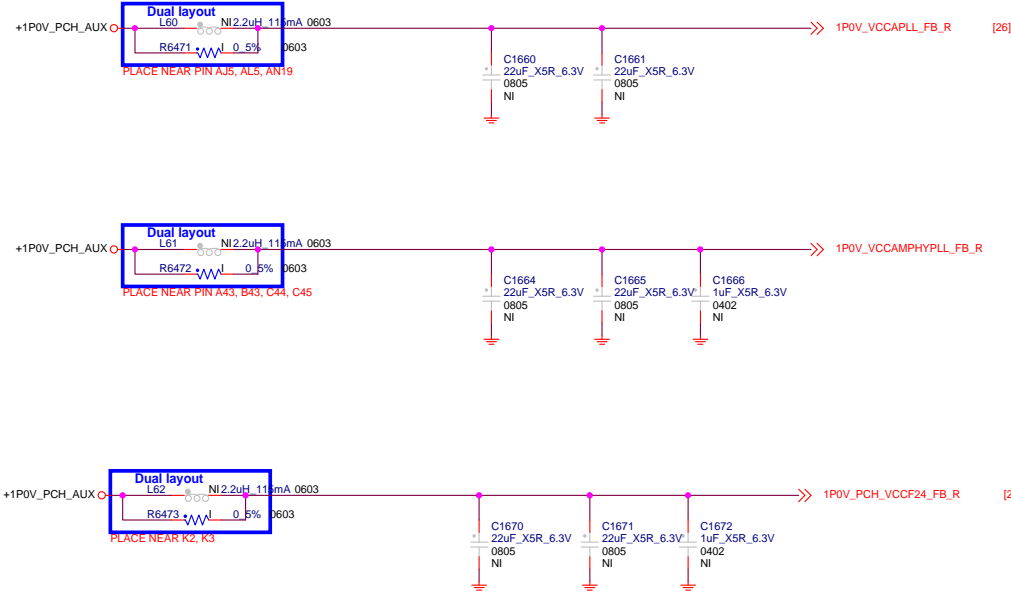


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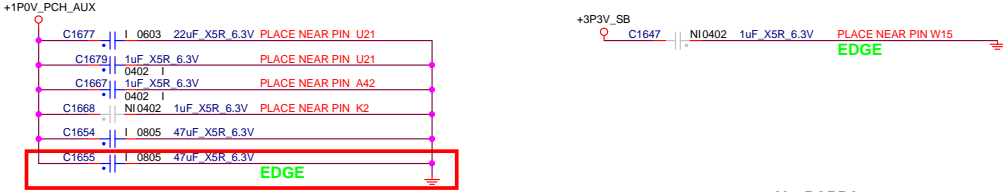
SKYLAKE Decoupling & filter

FILTER



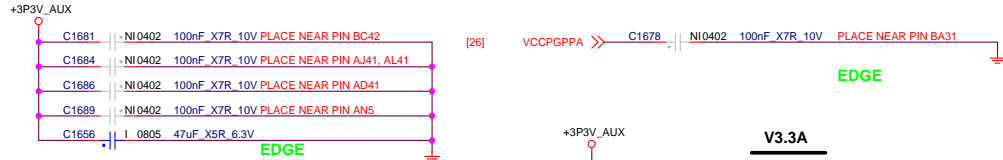
V1.0A

V3.3 DSW



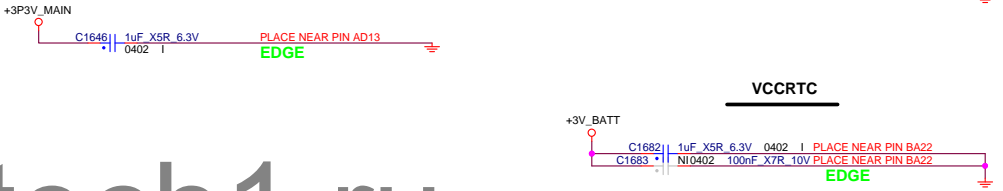
V1.8A / V3.3A

VccPGPPA

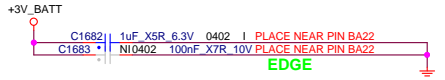


V1.8A / V1.8S / V3.3S

V3.3A



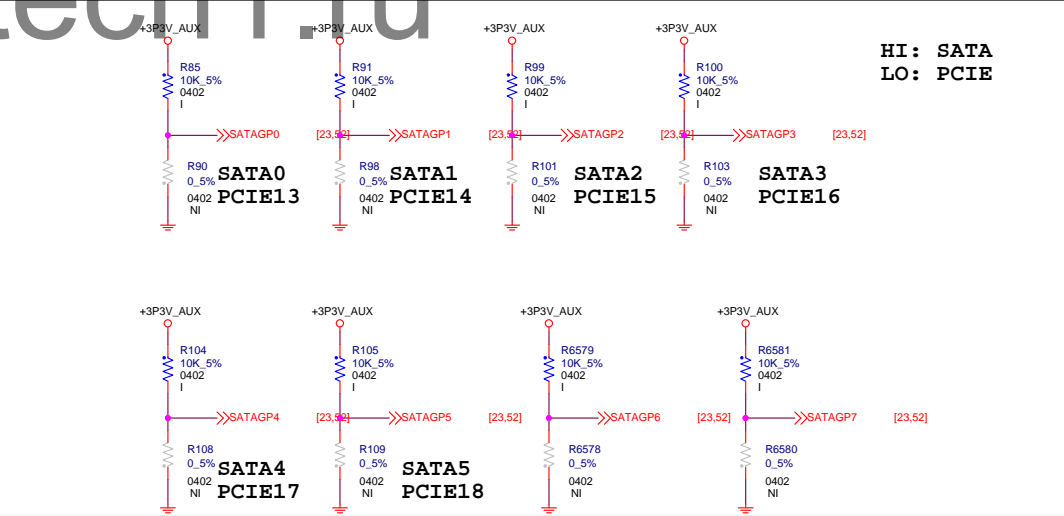
VCCRTC



Power Plane Isolation

Need to update for SLK

Voltage	Interface	PCH Pins sharing power rail
VCC_PCH 1.05V	Core	U26, U25, U23, U21, V26,
	PCIe/SATA/ USB3	T19, T20, P22, P23, P25, P26, P28, P14, P16, P17
	GPIO/LPC	AC12
	FDI	M14
	DIFFCLK	U12, V14 W14 AB2
	SSC	T16, V16 AA16, W16
PCH 3.3V Standby	USB2	AF19, AF20, AF22, AF23, AP22
	SUS	AM33, AN33
	USB2	AH18, AH20, AH22, AJ20, AK20
	AZALIA	AW26
	USB3	P20
PCH 3.3V	RTC	AP35
	CLK	AM7, AM9, AP5, AP7, AR4, AT5, AV4, AW4, AW9, AG12, AK11,
	HVCNOS	AG1
	PCIe	AV3, AW3
	Core	U30, W30
	Fuse	AF26



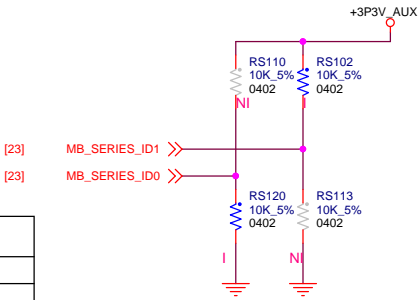
HI: SATA
LO: PCIE



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PCH		
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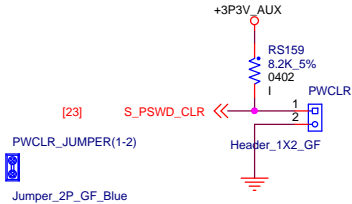
MB series ID

ID1	ID0	Type
0	0	SFF3
0	1	SFF5
1	0	SFF7
1	1	Farallon



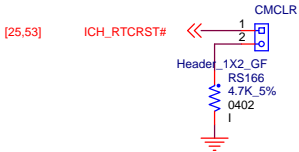
Clear Password

PASSWORD	SHORT : DEFAULT
	OPEN : CLEAR PASSWORD



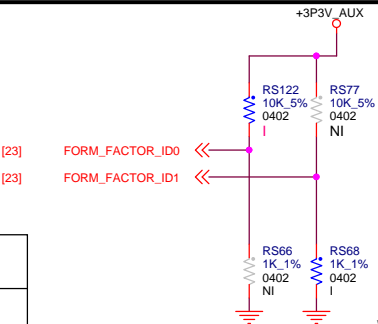
CLR_CMOS

CMOS	SHORT : CLEAR CMOS
	OPEN : DEFAULT

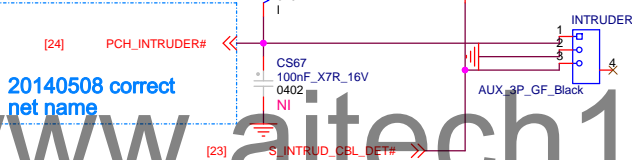


Form Factor ID

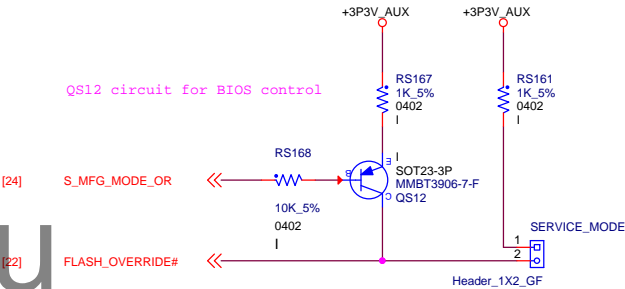
ID1	ID0	Type
1	1	MT
1	0	CT
0	1	SFF
0	0	Micro



Chassis Intruder



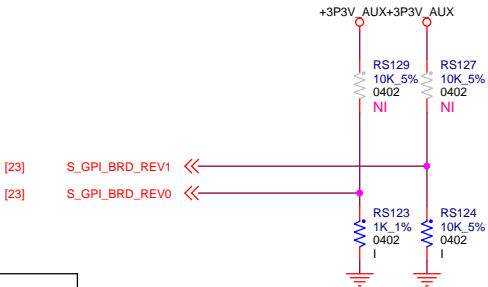
ME Disable (Flash override)



SERVICE_MODE	SHORT : ME DISABLE
	OPEN : DEFAULT

BOARD ID

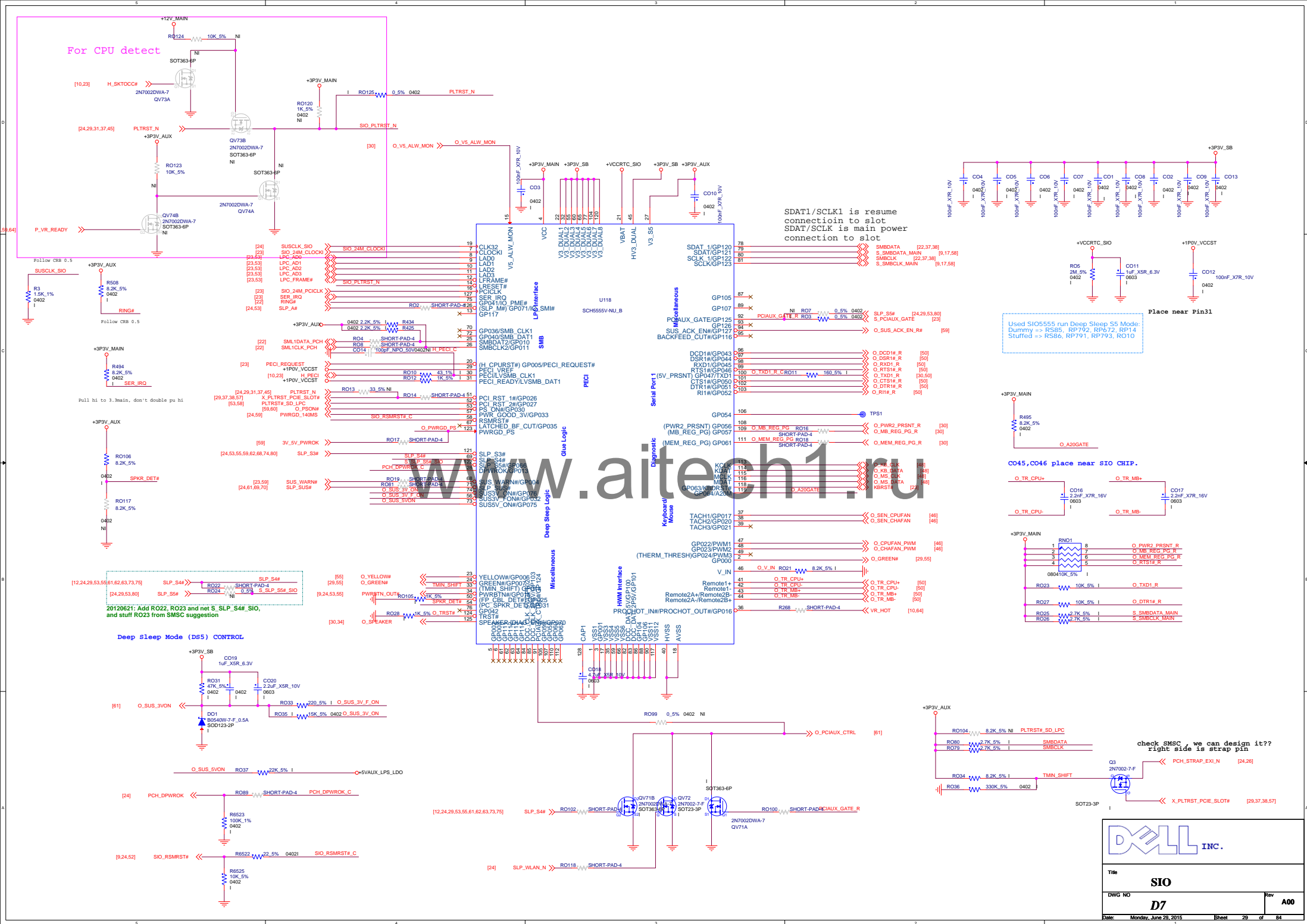
ID1	ID0	Type
1	1	X02
1	0	X01
0	1	X00
0	0	B00/A00



BEEP

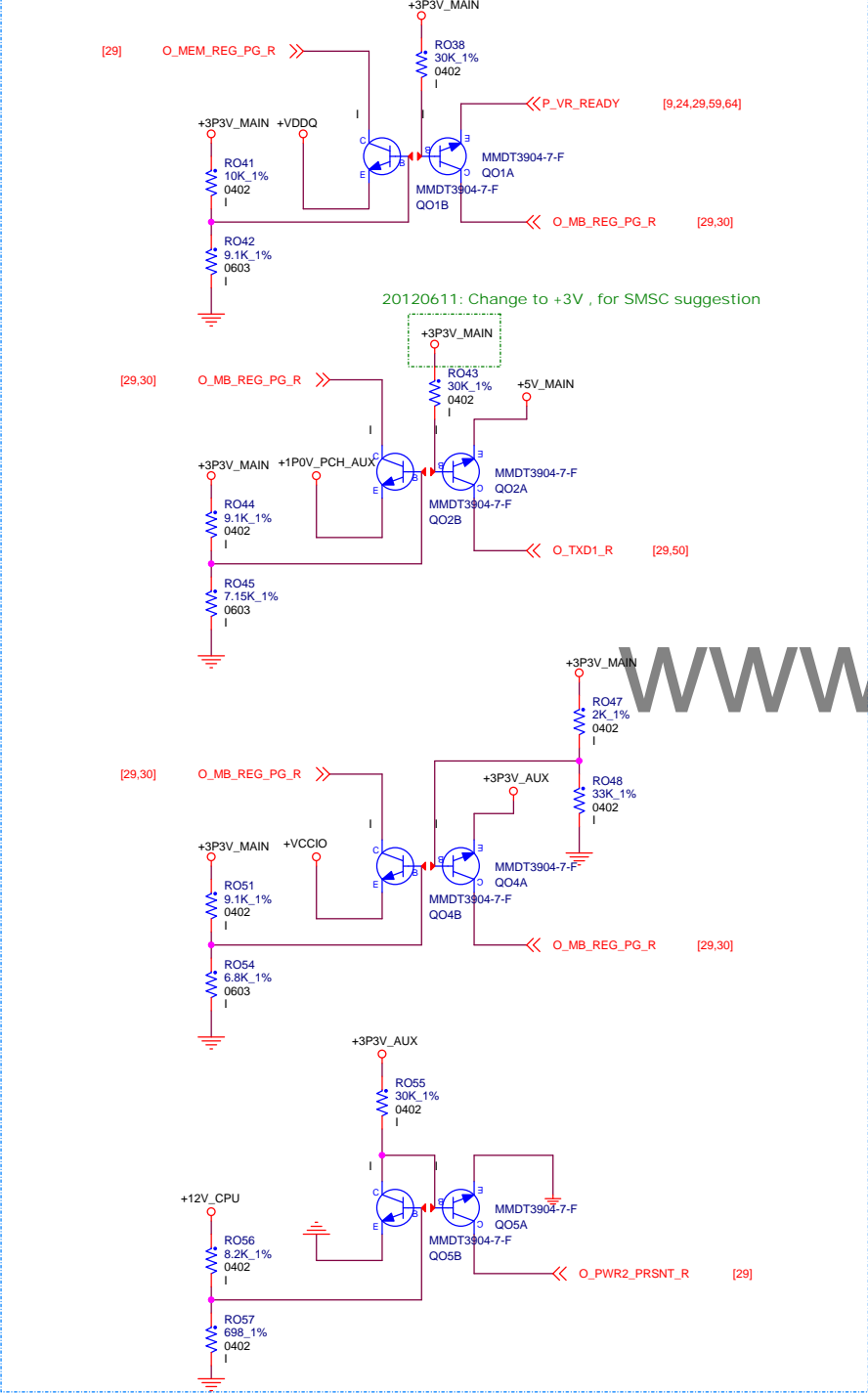


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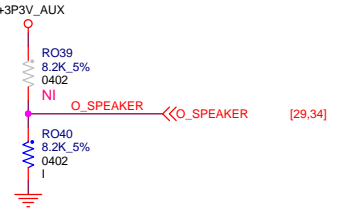


5555 PRE-POST DIAG Monitor

20140429 Chaned monitor power for SKYLAKE , MUST double confirm with SMSC

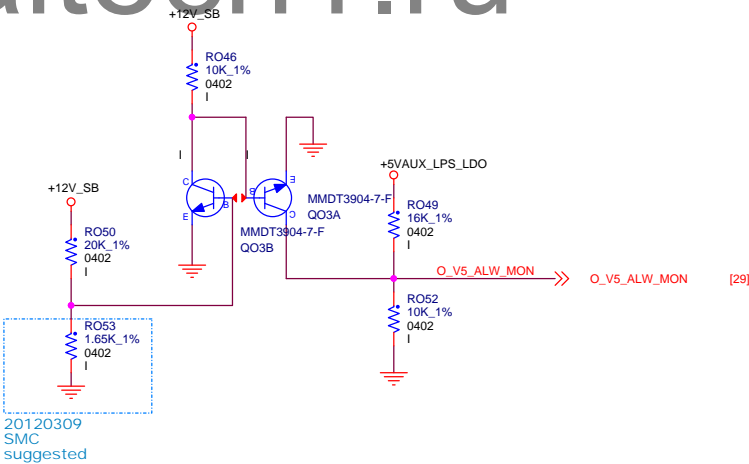


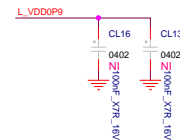
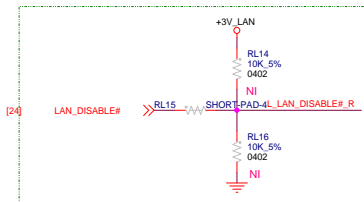
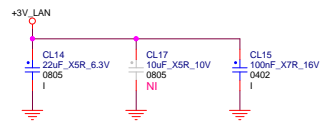
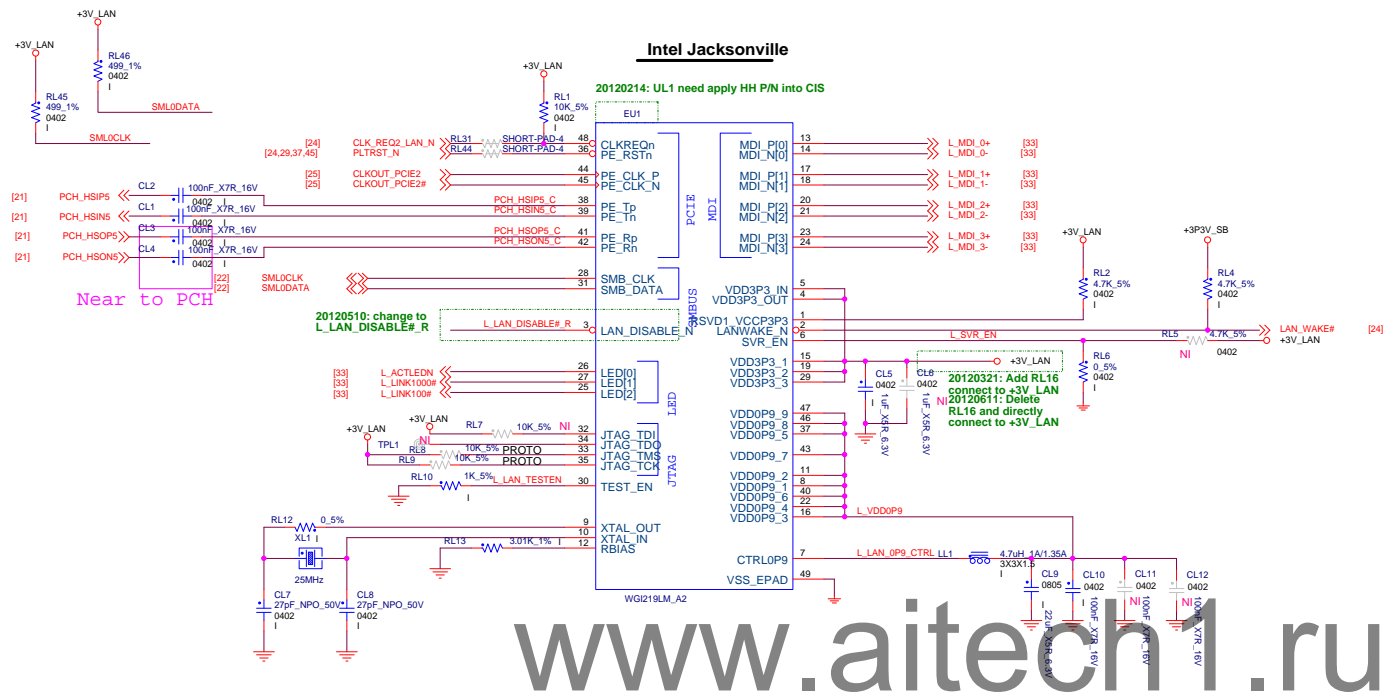
SIO STRAPING



SIO STRAPING	
	SPEAKER
	Diag_En
PULL HIGH	Disable
PULL LOW	Enable

SIO5555 V5_ALW Monitor






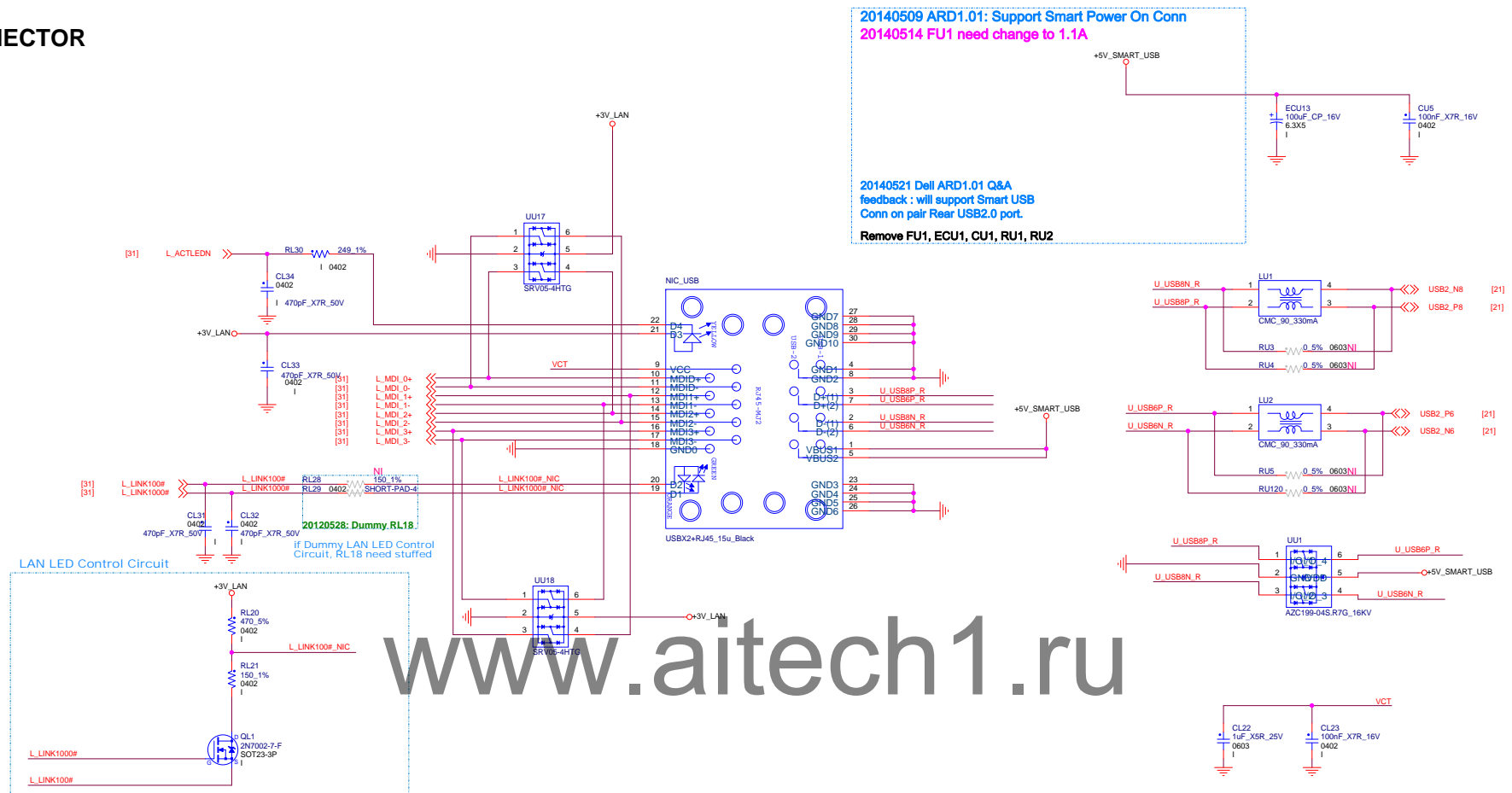
Intel PCH XDP Debug Connector

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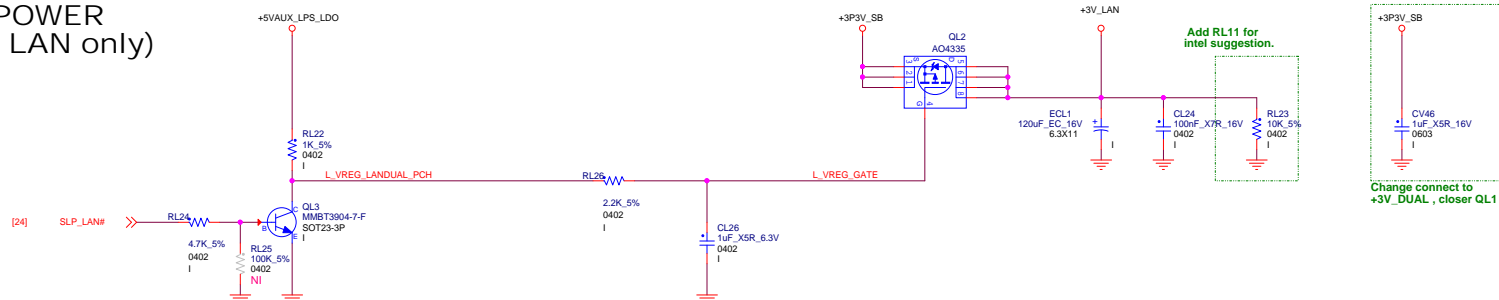
Project	
Spitfire	V
Scorpion	V
Toledo	V

 INC.	
Title	
CPU	
DWG NO	Rev
D7	A00
Date: Monday, June 29, 2015	
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LAN CONNECTOR



LAN POWER
(Intel LAN only)



Title

LAN

DWG NO	
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D7

Rev	A00
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Date: Monday, June 29, 2015

Sheet 33 of 84

20140507 Reserved +3.3V for AVDD2 for cost saving, but need REALTEK final report.

Layout: Close to codec

20140514 Realtek suggestion

Layout: Close to pin1

20140507 For TI chip 1.5V, this is template solution waiting CE for final solution suggestion

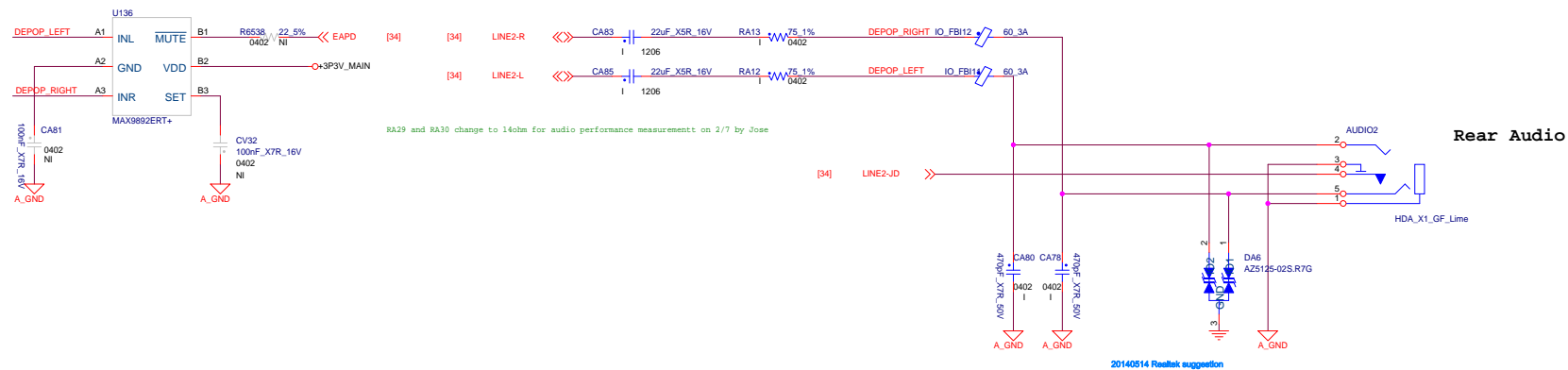
201405012 Follow DC use 5325, waiting confirm CE for final solution suggestion

$$V_{out} = 0.8 * (1 + RK33 / RK35) = 1.52V$$

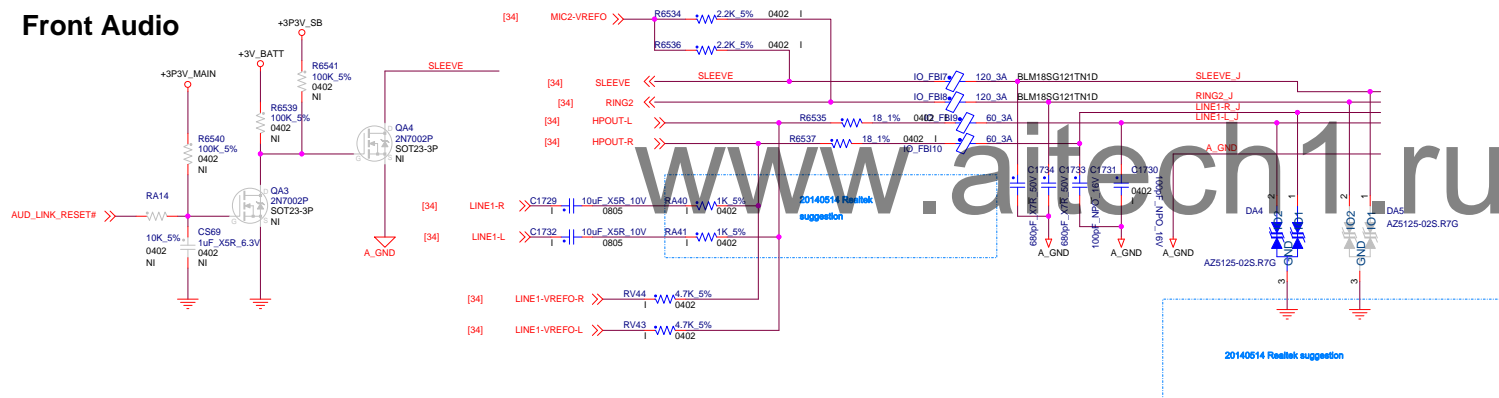
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20140514 Realtek suggestion: If mobile-HDA link used 1.8V power domain, please reserve a level shift circuit.

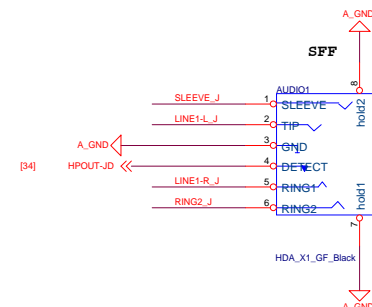
Rear Audio Jack



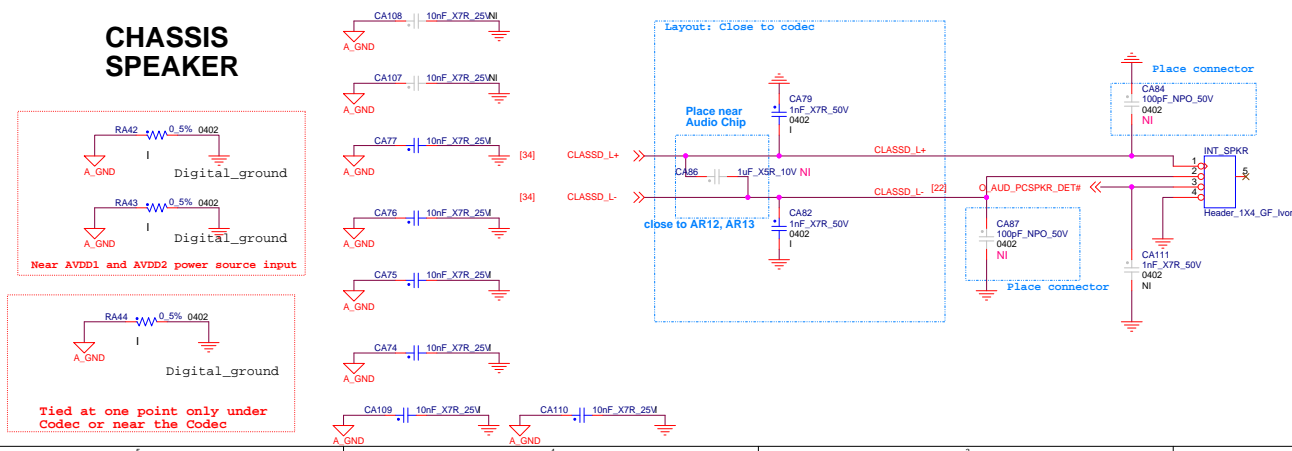
Front Audio



Front Panel



CHASSIS SPEAKER




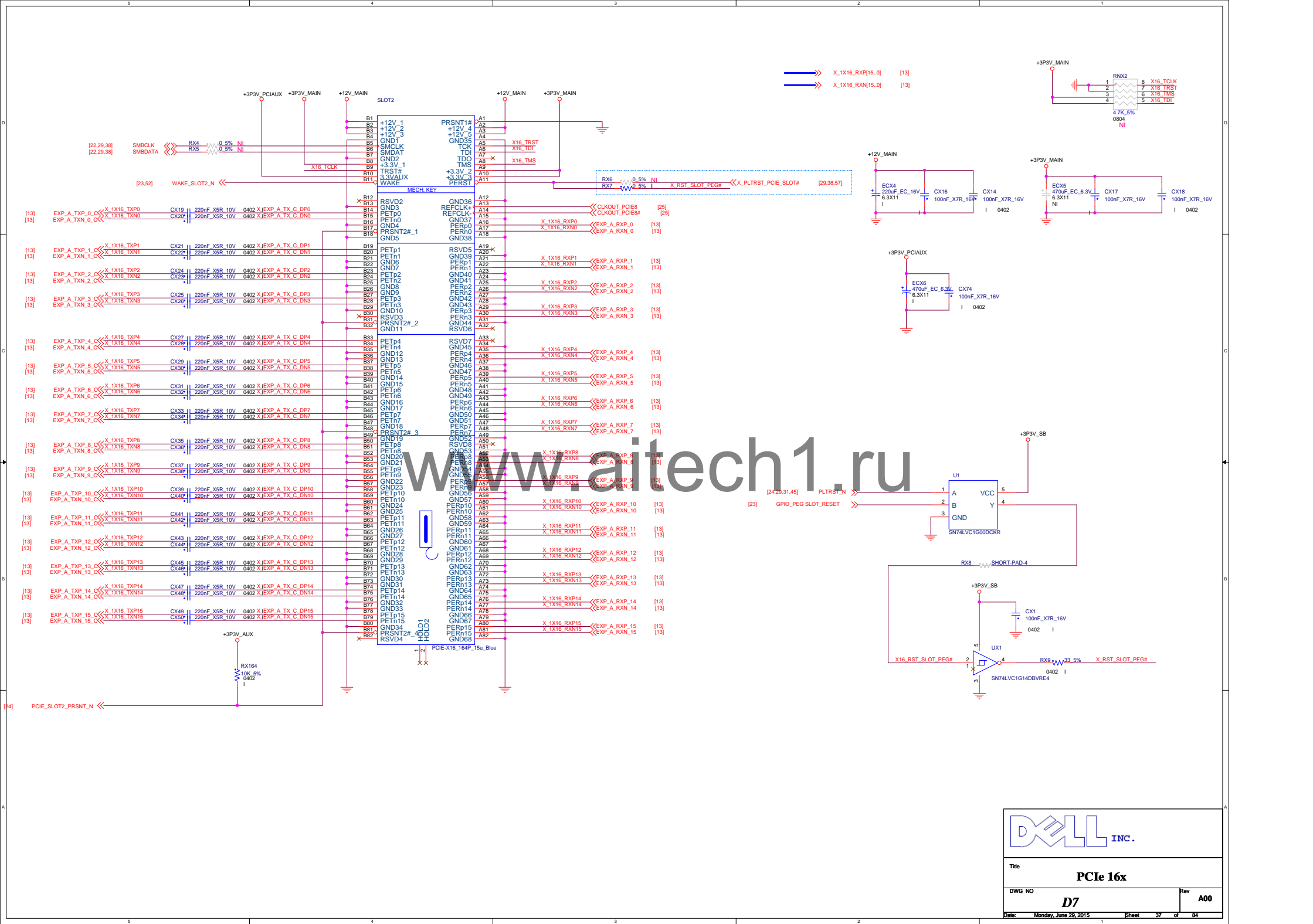
Title		AUDIO	
DWG NO		Rev	
<i>D7</i>		A00	
Date:	Monday June 20 2016	Sheet	3K of 34

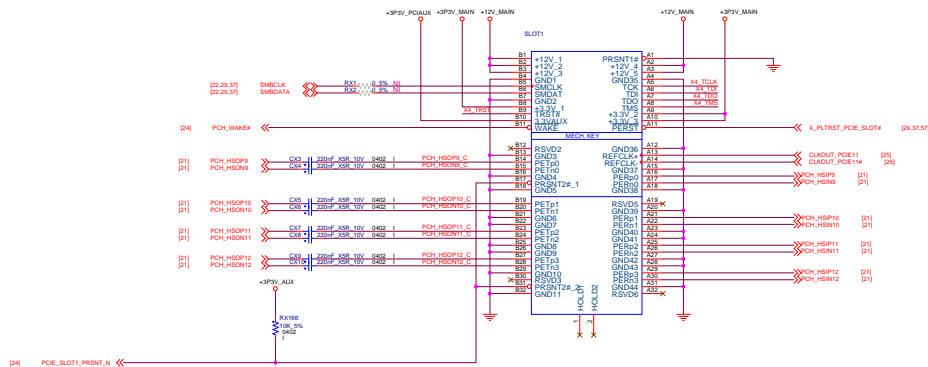
Intel PCH XDP Debug Connector

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Project	
Spitfire	V
Scorpion	V
Toledo	V

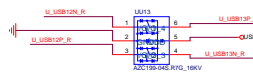
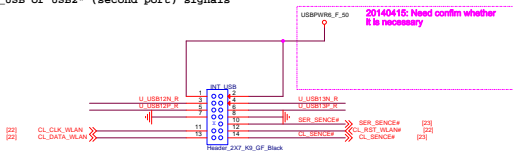
 INC.	
Title	
CPU	
DWG NO	Rev
D7	A00
Date: Monday, June 29, 2015	
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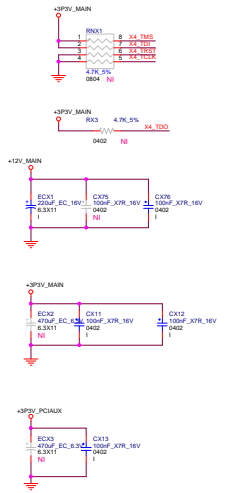
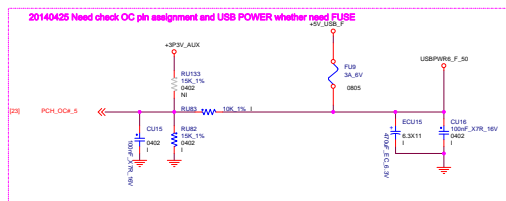
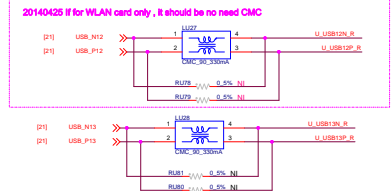


14 pin USB/CLINK Header				
+5V_USB	1	2	+5V_USB	
USB1N	3	4	USB2N	
USB1P	5	6	USB2P	
GND	7	8	GND	
Key (no pin)	9	10	SER_SENSE	
CLINK_CLK	11	12	CLINK_RST	
CLINK_DAT	13	14	CL_SENSE	

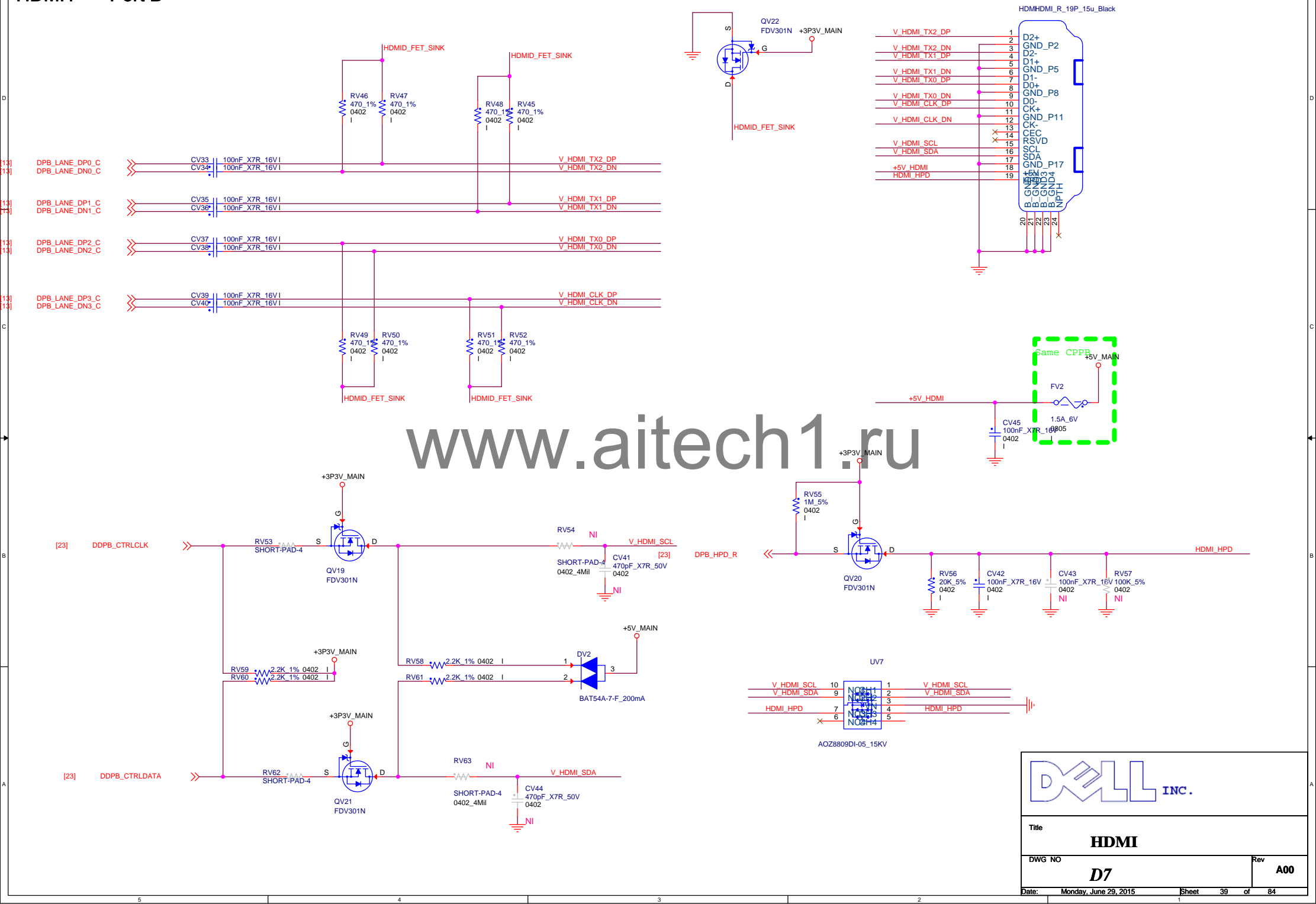
ARD 0.9 :Header populated on 7/9 series only
 Provides vPro and BT support from Intel wireless Add-in-Card
 USB and CLINK signals passed on cable from motherboard to Add-in-Card
 Compatible with standard USB 2.0 headers and cables
 14 pin non shrouded header 0.1 pin spacing,
 Pin 14 allows sense of the CLINK/BT cable ,
 Add-in-Card does not use +5V_USB or USB2* (second port) signals




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HDMI1 --> Port B



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**INC.**

Title

HDMI

DWG NO

D7

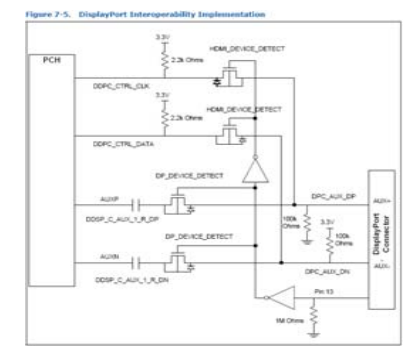
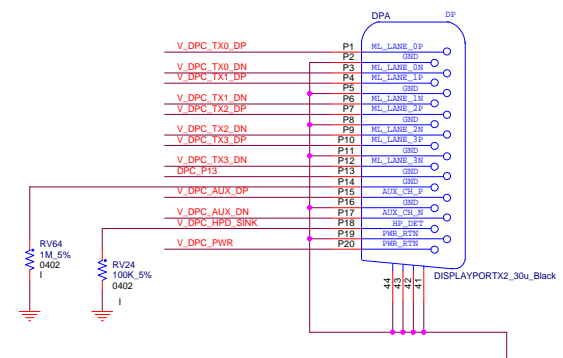
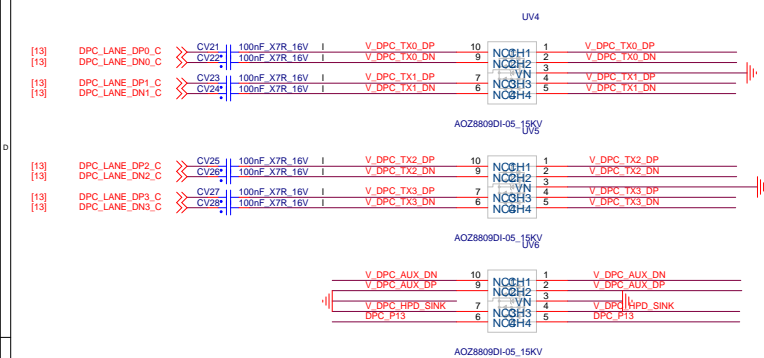
Date: Monday, June 29, 2015

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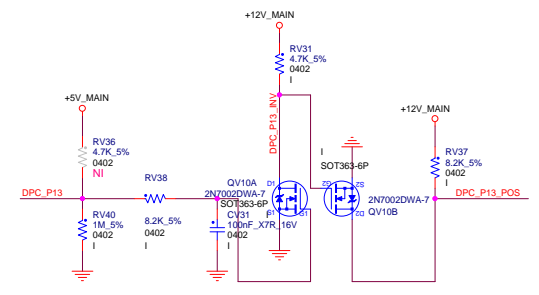
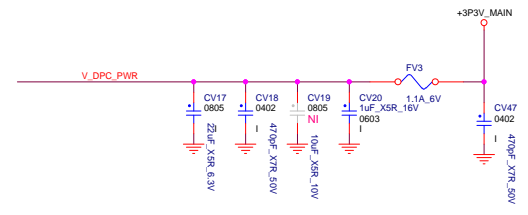
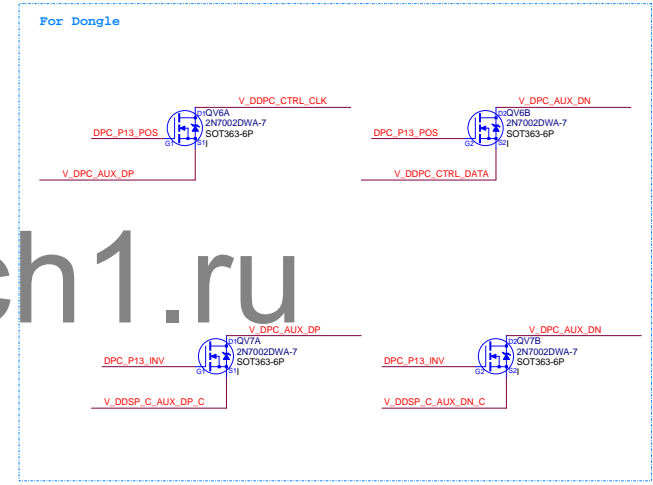
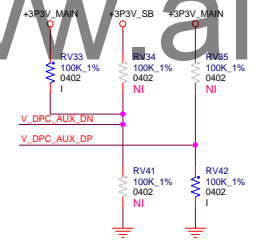
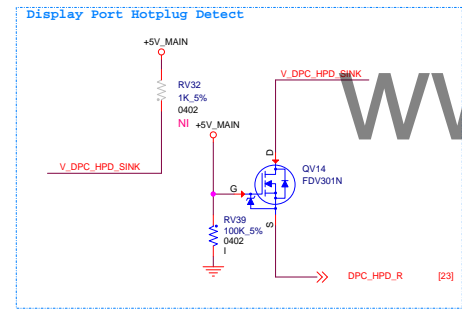
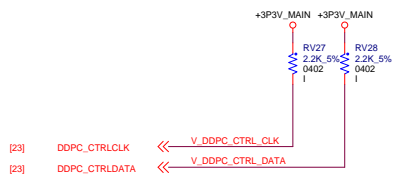
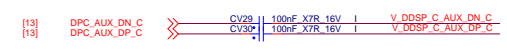
Rev

A00

DP --> Port C

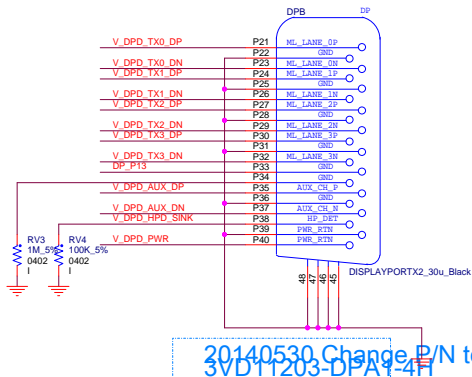
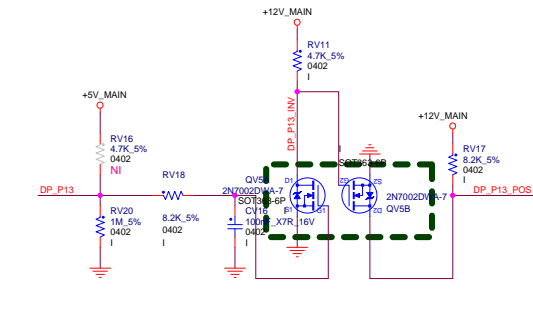
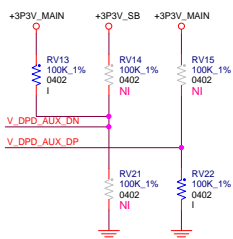
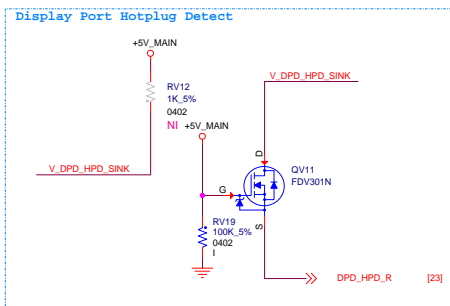
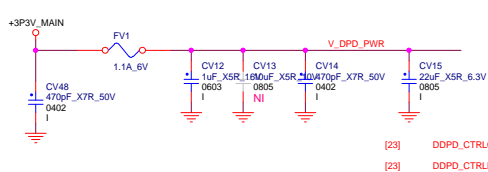
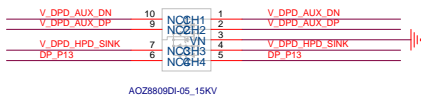
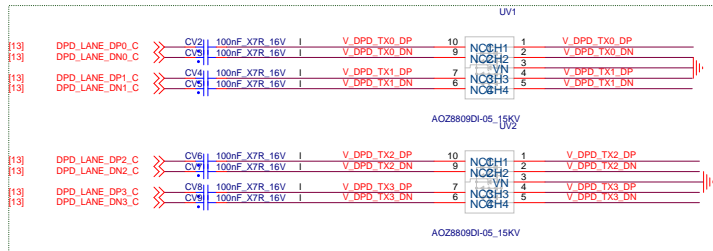


30140530 Change P/N to 1203-DPA9-4H



DP → Port D

20120521: Delete UV4 · UV1, UV2, UV3 change to INFINEON_ESD3V3U4ULC



20140530 Change P/N to 3VD11203-DPA1-4H

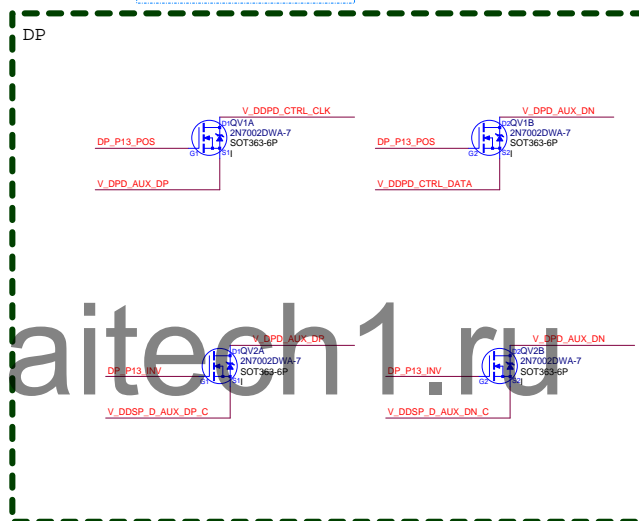


Figure 7-5. DisplayPort Interoperability Implementation

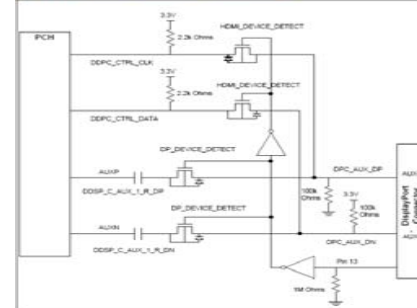
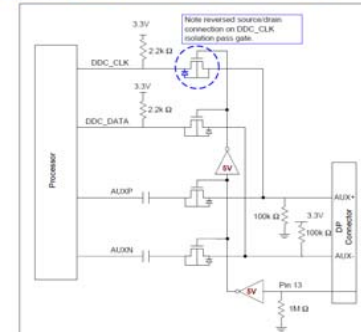
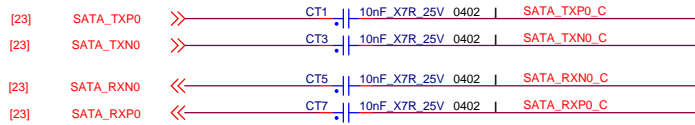
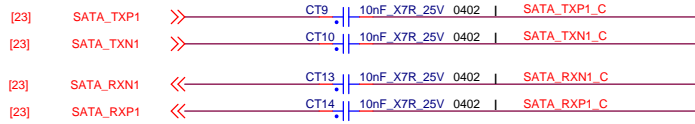
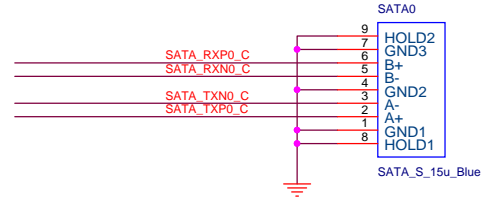


Figure 5-11. DisplayPort* Auxiliary Channel Dual Mode Support Protection Circuit

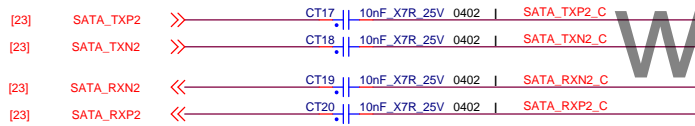
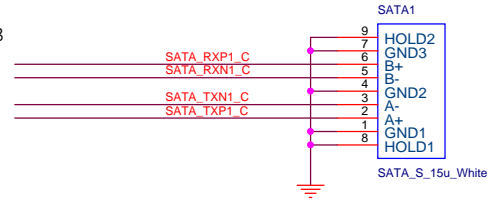




Blue SATA3

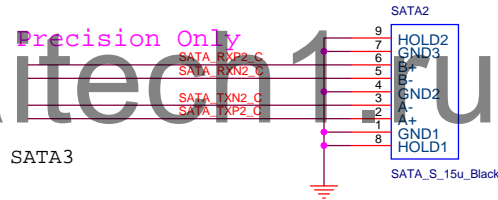


white ODD SATA3



SFF7/5 and Precision Only

Black SATA3



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20140505 ARD0.92: Each pair of USB ports will be current limited to 2.5A

20140505 ARD0.92: Each pair of USB ports will be current limited to 2.5A

201405014 Reserved for VDROP TEST


201405014 Reserved for VDROP TEST



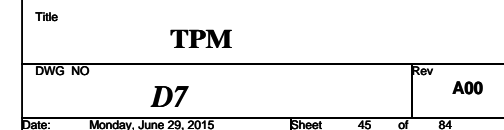
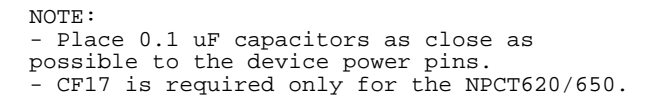
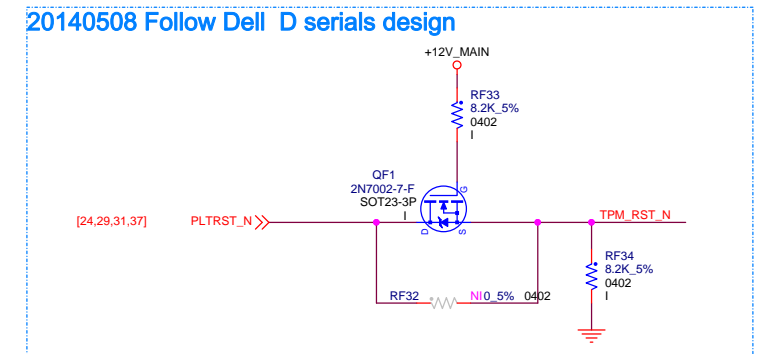
Intel PCH XDP Debug Connector

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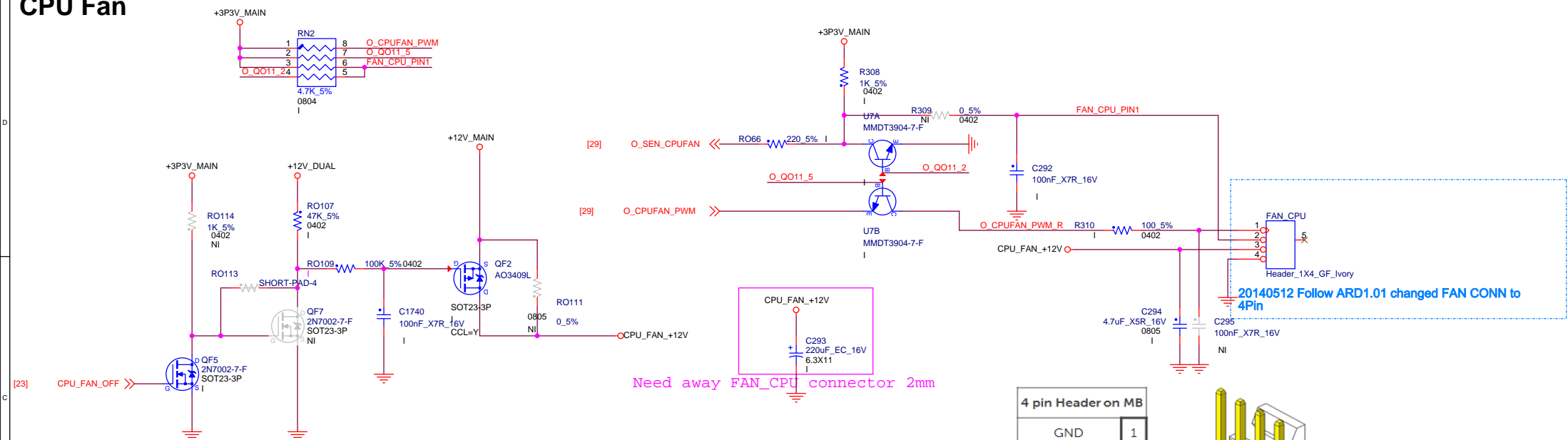
Project	
Spitfire	V
Scorpion	V
Toledo	V

 INC.	
Title	
CPU	
DWG NO	Rev
D7	A00
Date: Monday, June 29, 2015	
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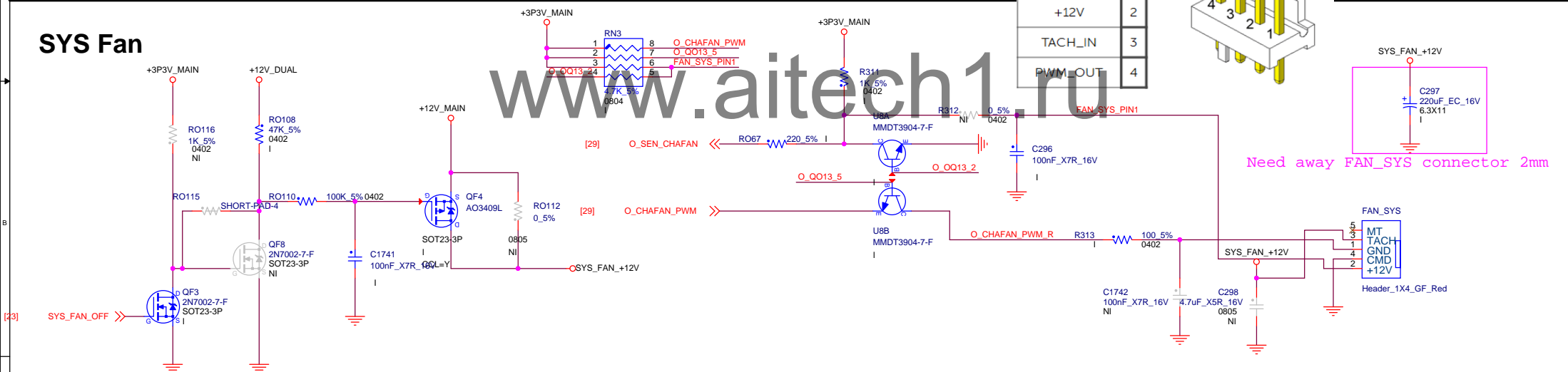
HW Low Power Mode	RF62	RF63	RF60
Support	Un-stuff	Stuff	Stuff
Not support	Stuff	Un-stuff	Un-stuff



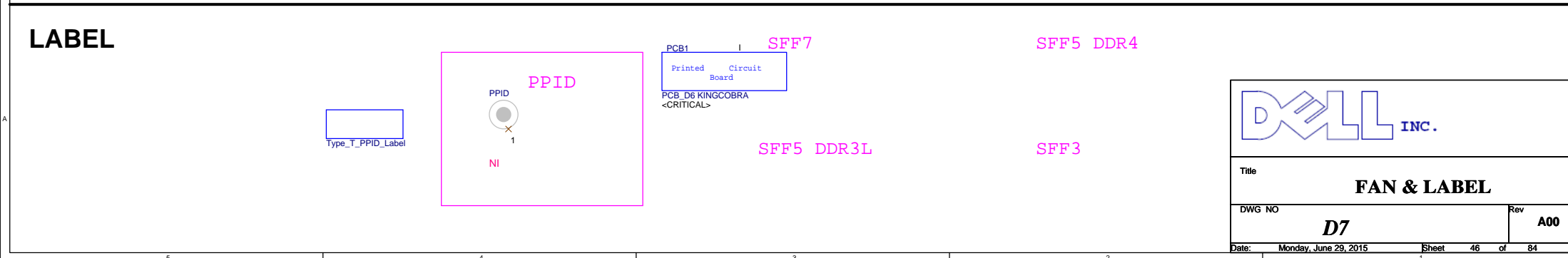
CPU Fan



SYS Fan




LABEL

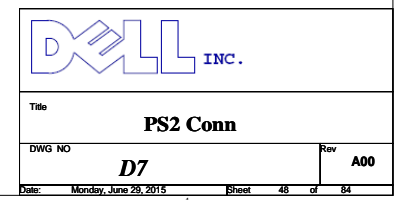


Intel PCH XDP Debug Connector

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Project	
Spitfire	V
Scorpion	V
Toledo	V


 INC.	
Title	
CPU	
DWG NO	Rev
D7	A00
Date: Monday, June 29, 2015	
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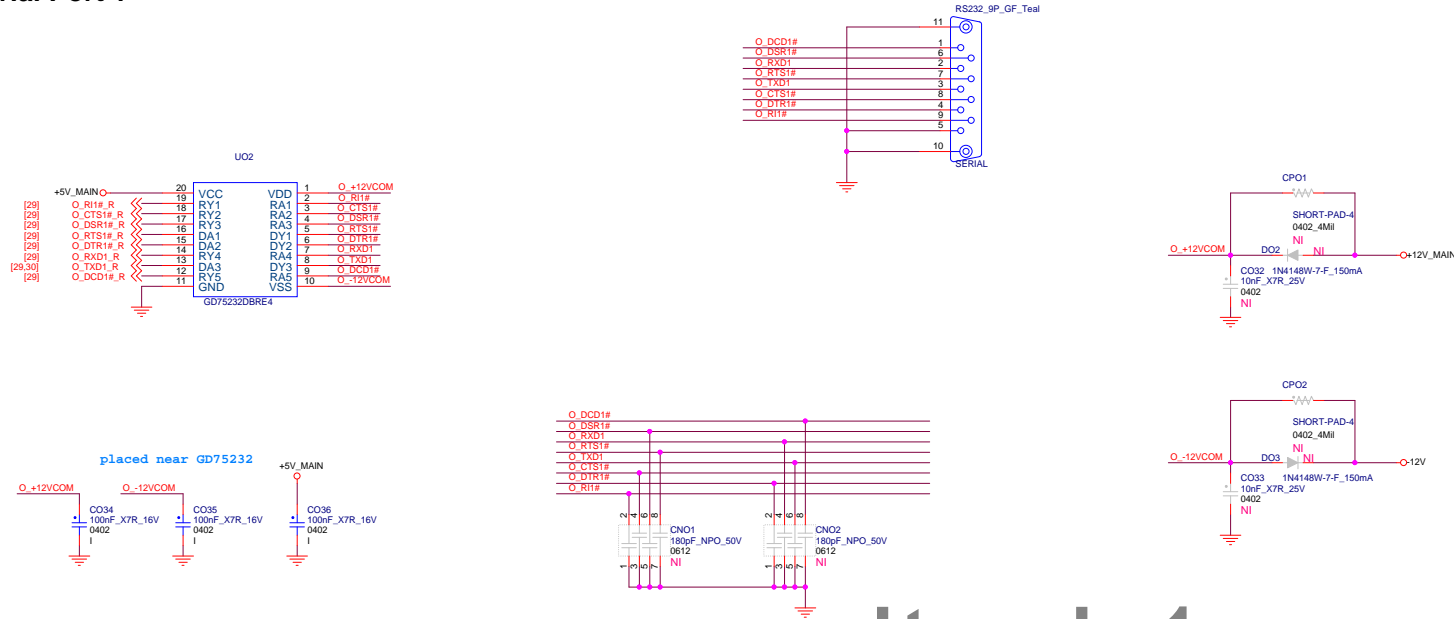
Intel PCH XDP Debug Connector

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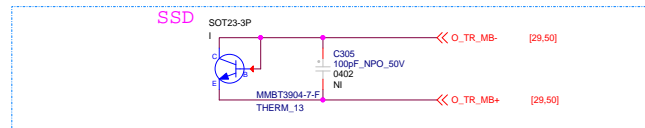
Project	
Spitfire	V
Scorpion	V
Toledo	V

 INC.	
Title	
CPU	
DWG NO	Rev
D7	A00
Date: Monday, June 29, 2015	
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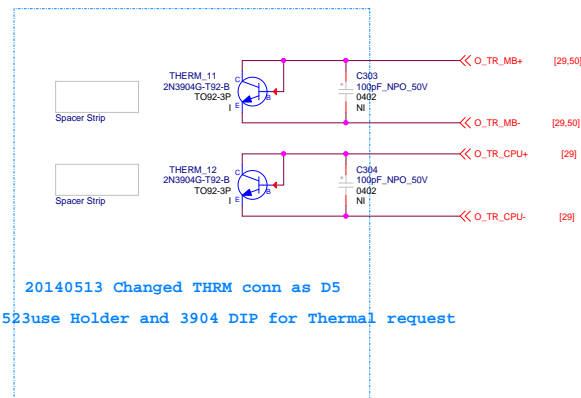
Serial Port 1

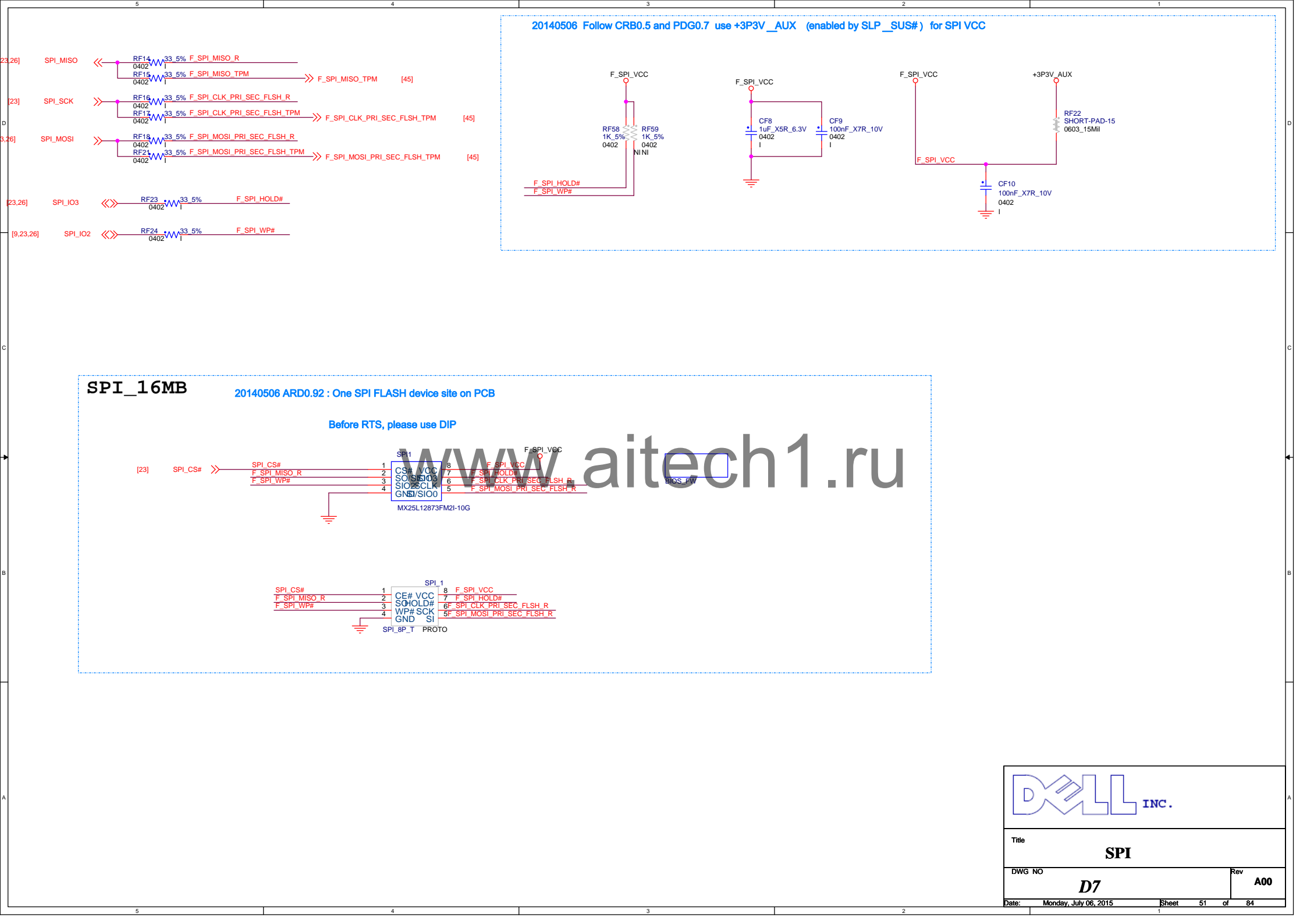


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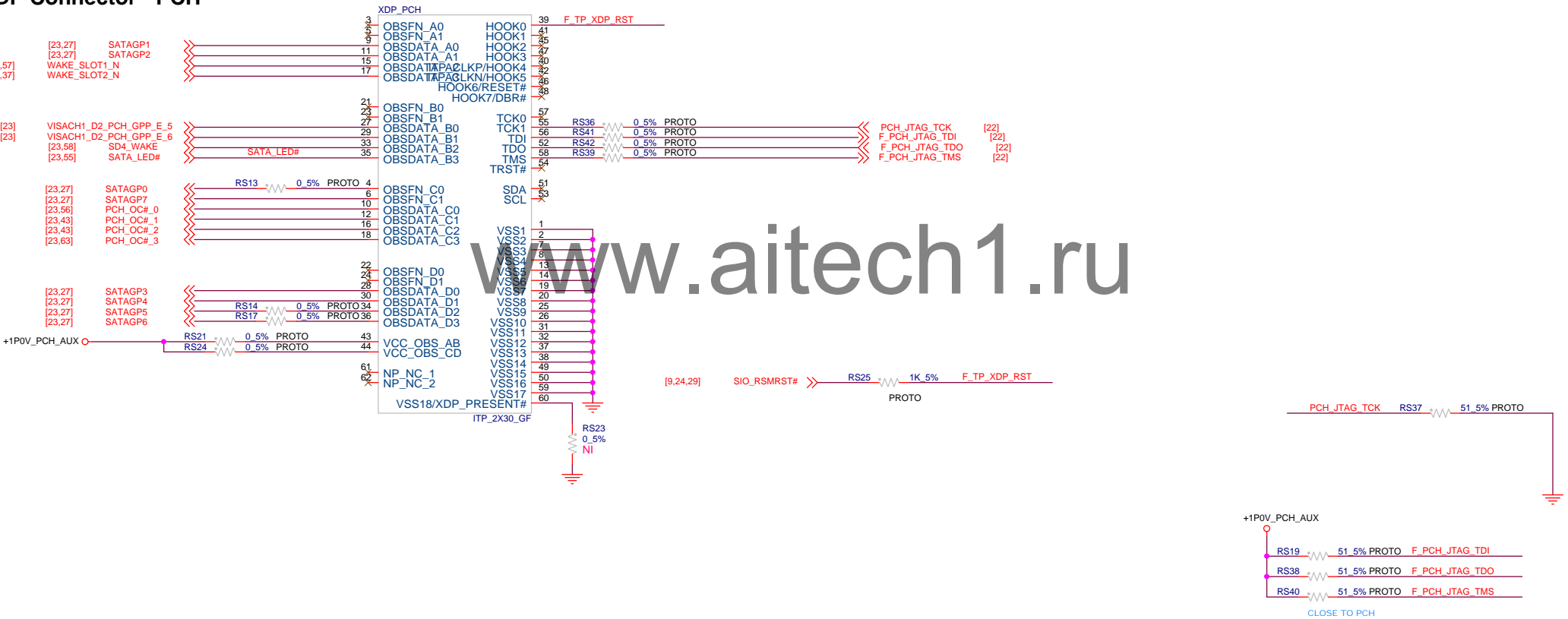


Thermal Header





20140505 Remove Duplicated XDP



Title

XDP

DWG NO

D7

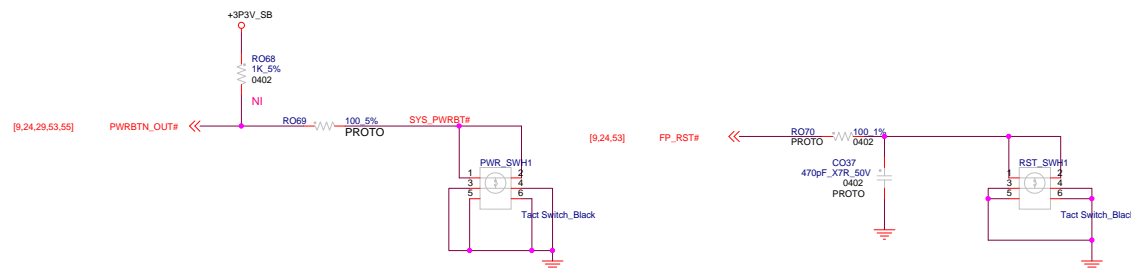
Rev

A00

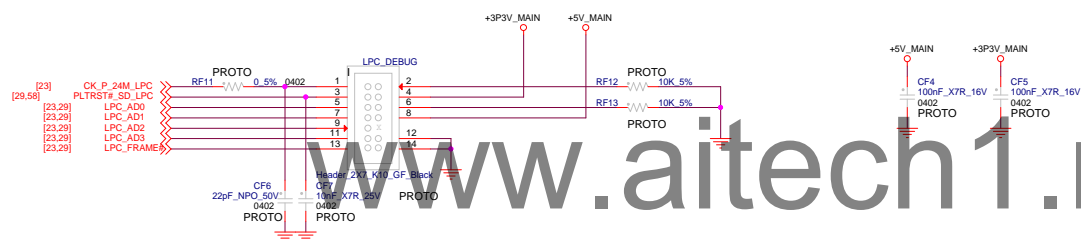
Date: Monday, June 29, 2015

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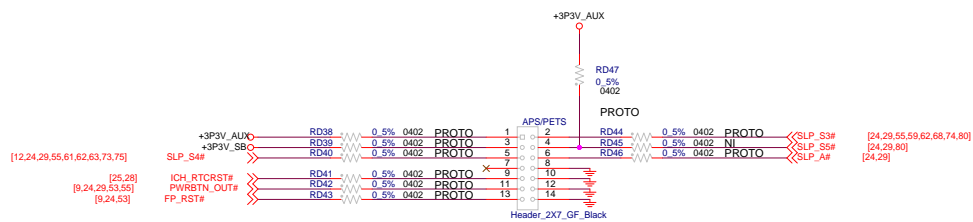
Reset Bottom



LPC DEBUG



APS Debug



Desktop		
APS Connector	Pin	Meaning
Pin 1	VccSut3_3	3.3 V Suspend Power Well
Pin 2	SLP_5#	When asserted (0) system is in S3
Pin 3	VccDSW3_3	Used to determine if system is in Deep S3
Pin 4	VccSut3_3	When off (0) system is in S5
Pin 5	SLP_5#	When asserted (0) system is in S4
Pin 6	SLP_4#	When asserted (0) ME is in Moff
Pin 7		Unused
Pin 8	GND	Ground
Pin 9	RTCST#	When asserted (0) CMOS is cleared
Pin 10	GND	Ground for RTCST#
Pin 11	PWRBTN#	When asserted (0) Power Button Pushed
Pin 12	GND	Ground for PWRBTN#
Pin 13	SYS_RESET#	When asserted (0) Reset Button Pushed
Pin 14	GND	Ground for SYS_RESET#



Title

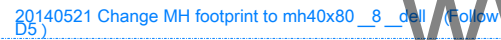
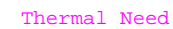
Pilot Run Conn

DWG NO	
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D7

Rev A00

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Tide

EMI

DWG NO	
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Rev	A00
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Date: Monday, June 29, 2015

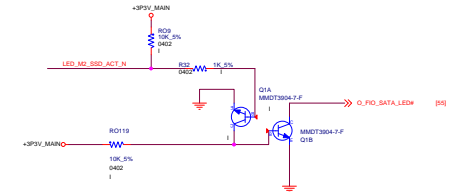
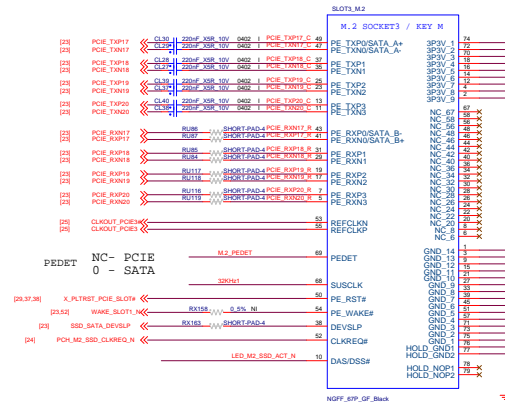
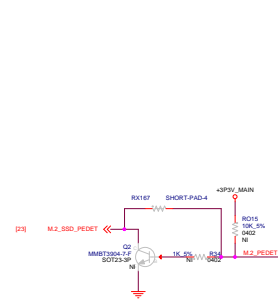
Sheet 54 of 84

SFF

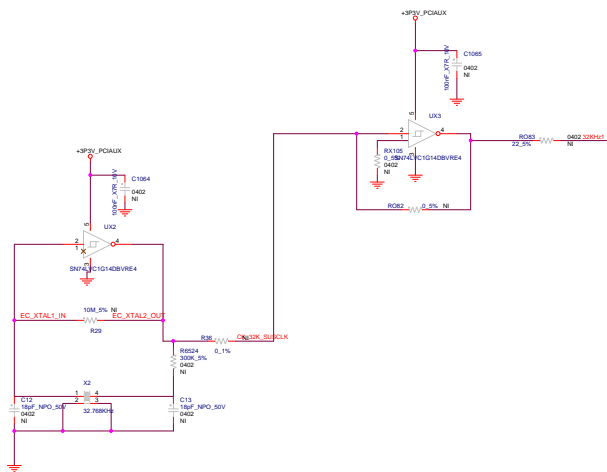


DWG NO	Rev
<i>D7</i>	A00

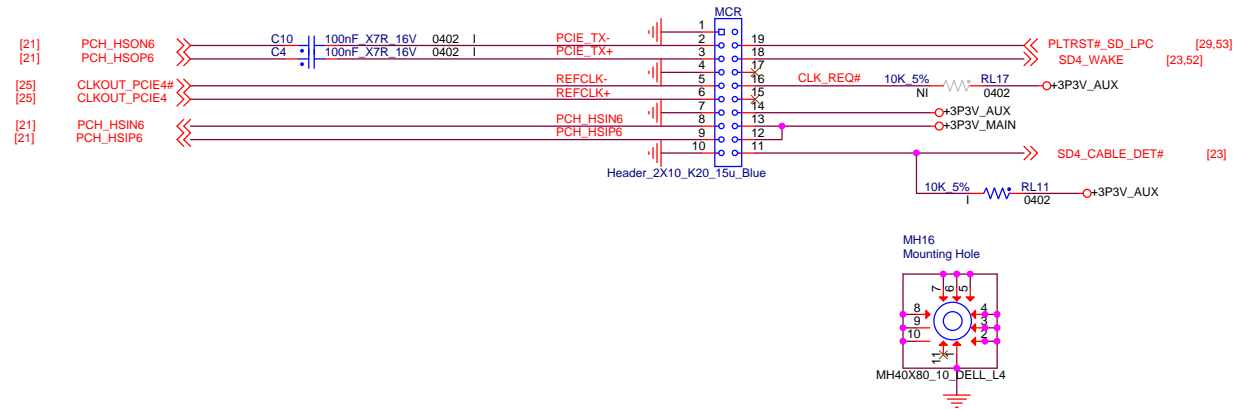
Date: Monday, June 29, 2015 Sheet 56 of 84



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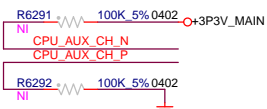
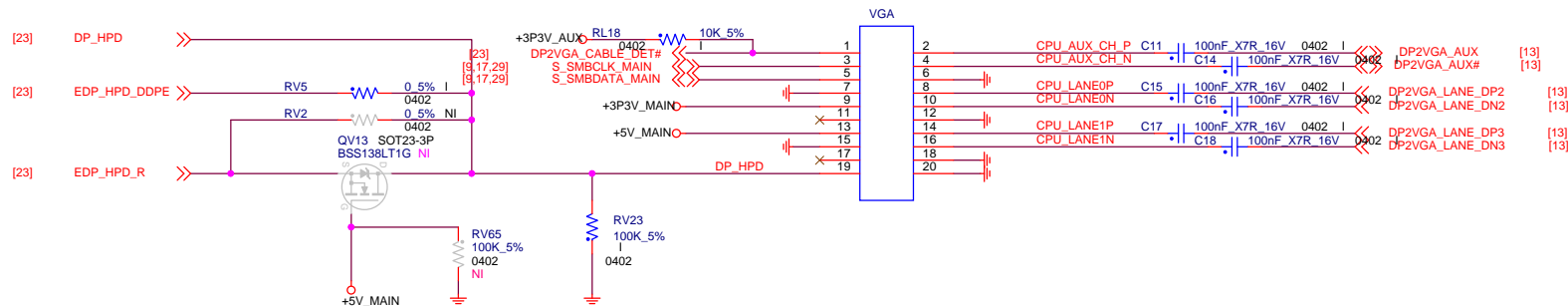


SD4.0 CONN



eDP to VGA CONN
M/B part already OK

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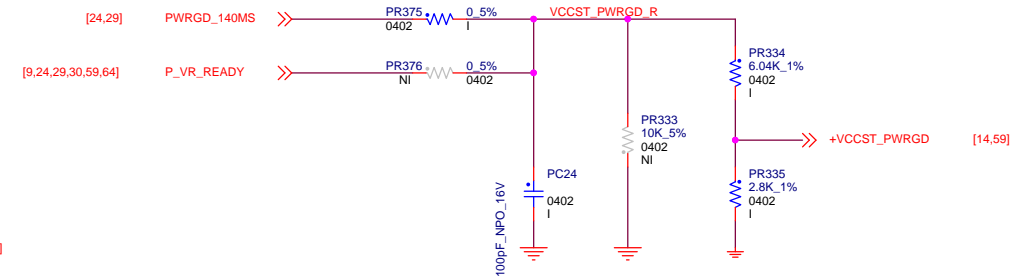
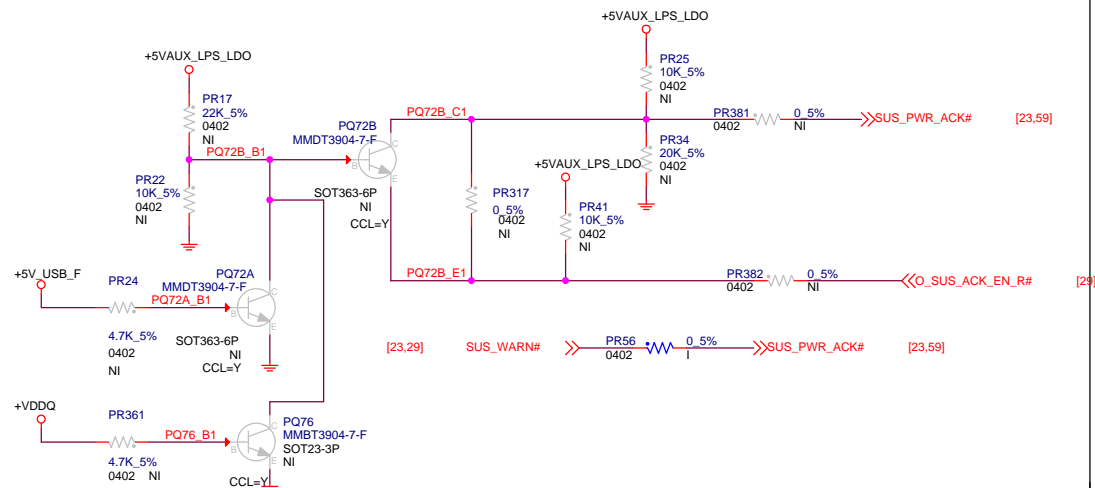


20140515 reserved for AUX

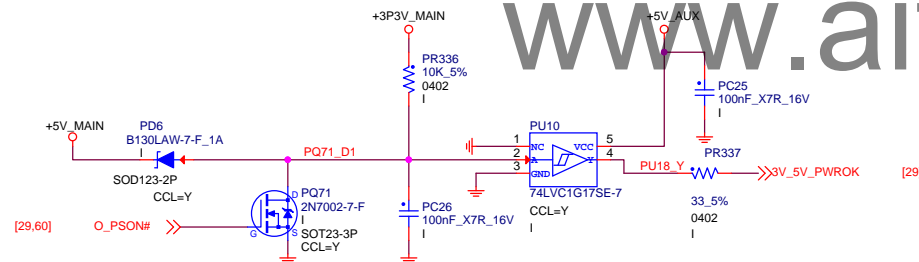


Title		
SD4.0 CON/ DP TO VGA CON		
DWG NO	Rev	
D7	A00	
Date: Monday, June 29, 2015	Sheet 58	of 84

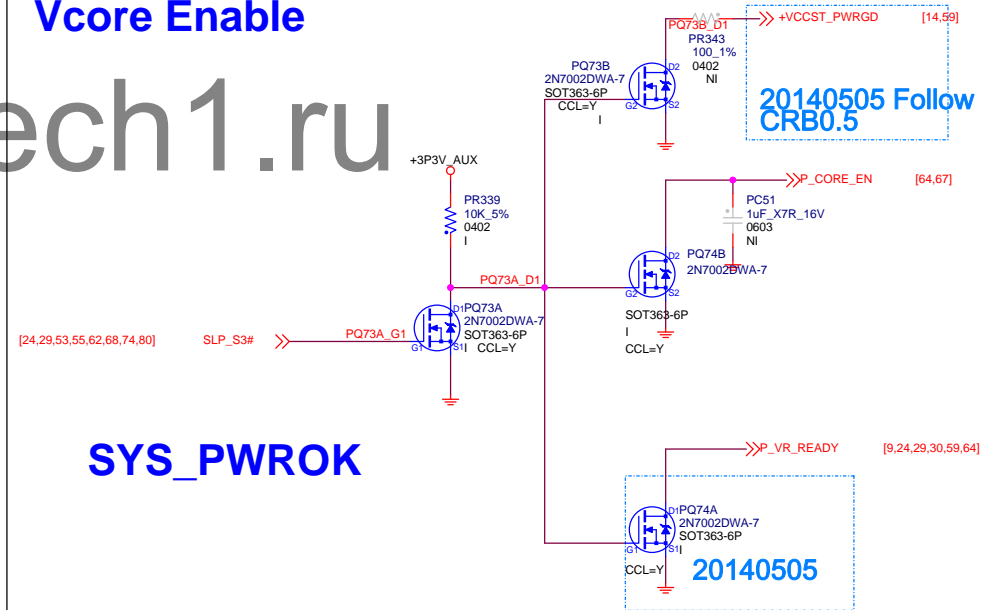
VCCST_PWRGD/PCH_PWROK



Power Sequence



Vcore Enable



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Power Sequence

DWG NO

D7

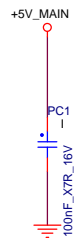
Rev

A00

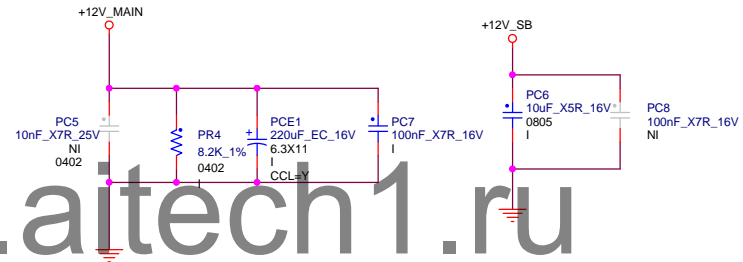
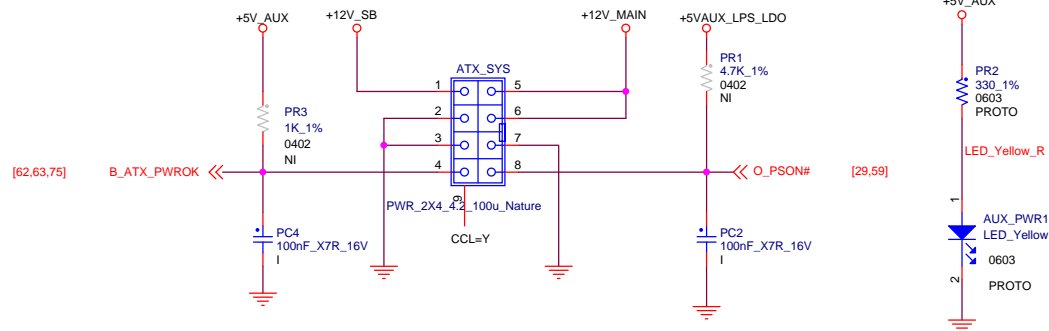
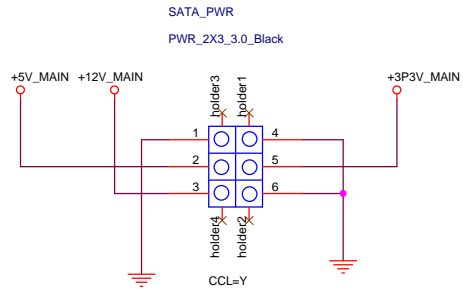
Date: Monday, June 29, 2015

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ATX POWER CONNECTOR



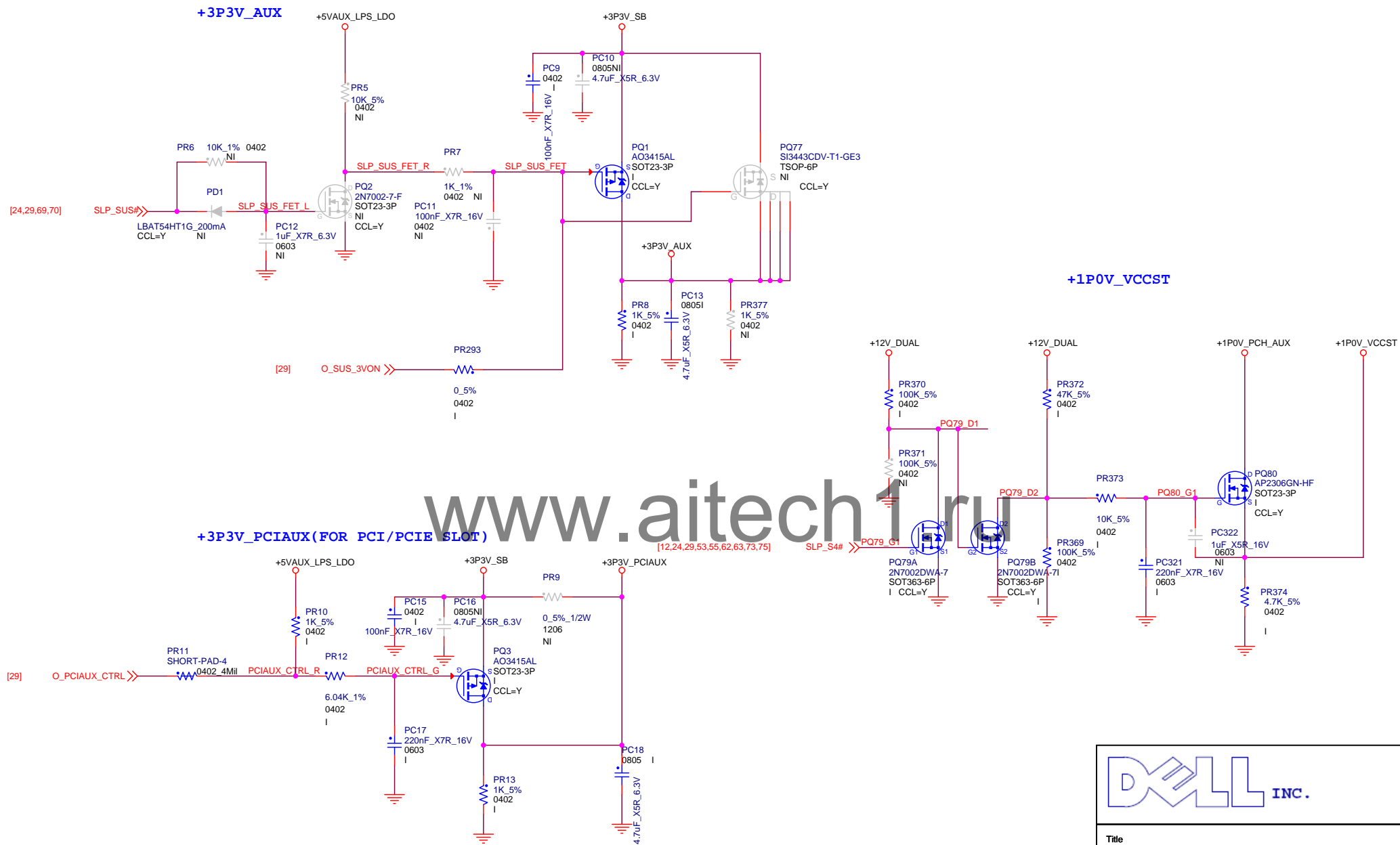
For ODD and HDD For SFF



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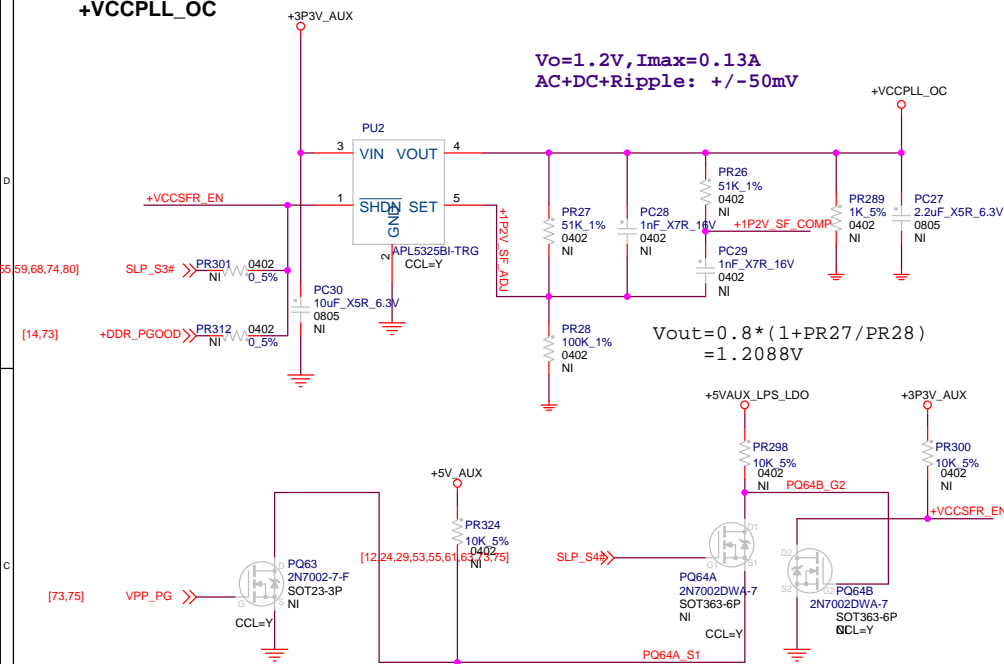


Title		
Power CONN		
DWG NO	Rev	A00
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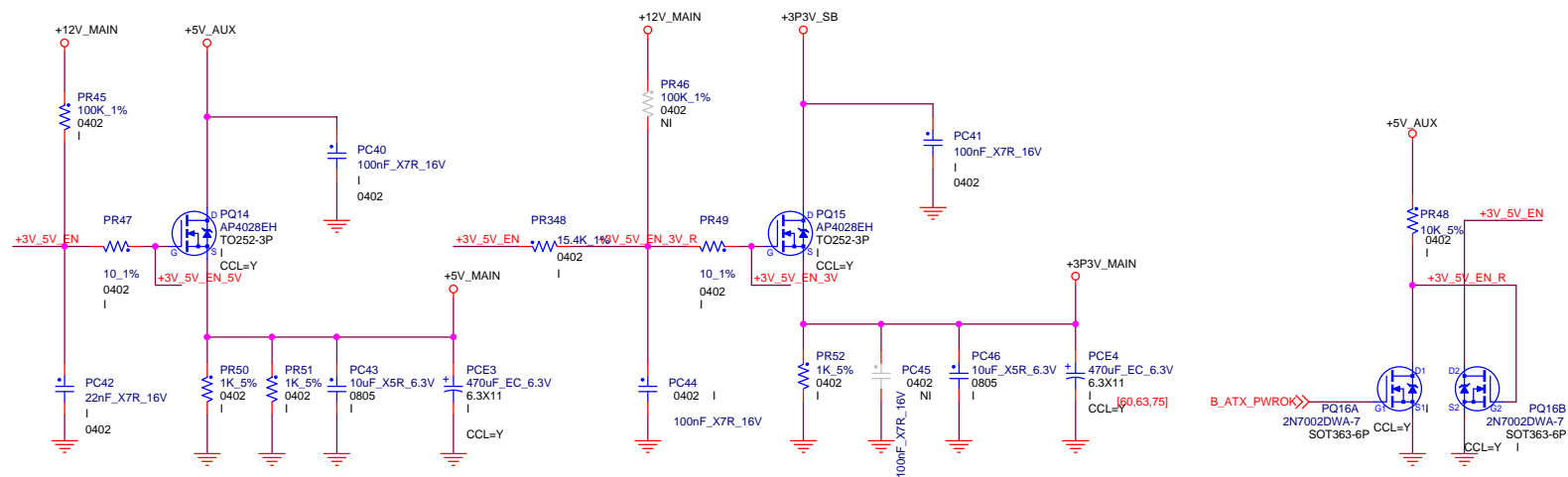
Title		
Power-1: Linear Power-1		
DWG NO		Rev
D7		A00
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+VCCPLL_OC



+5V MAIN

+3P3V_MAIN

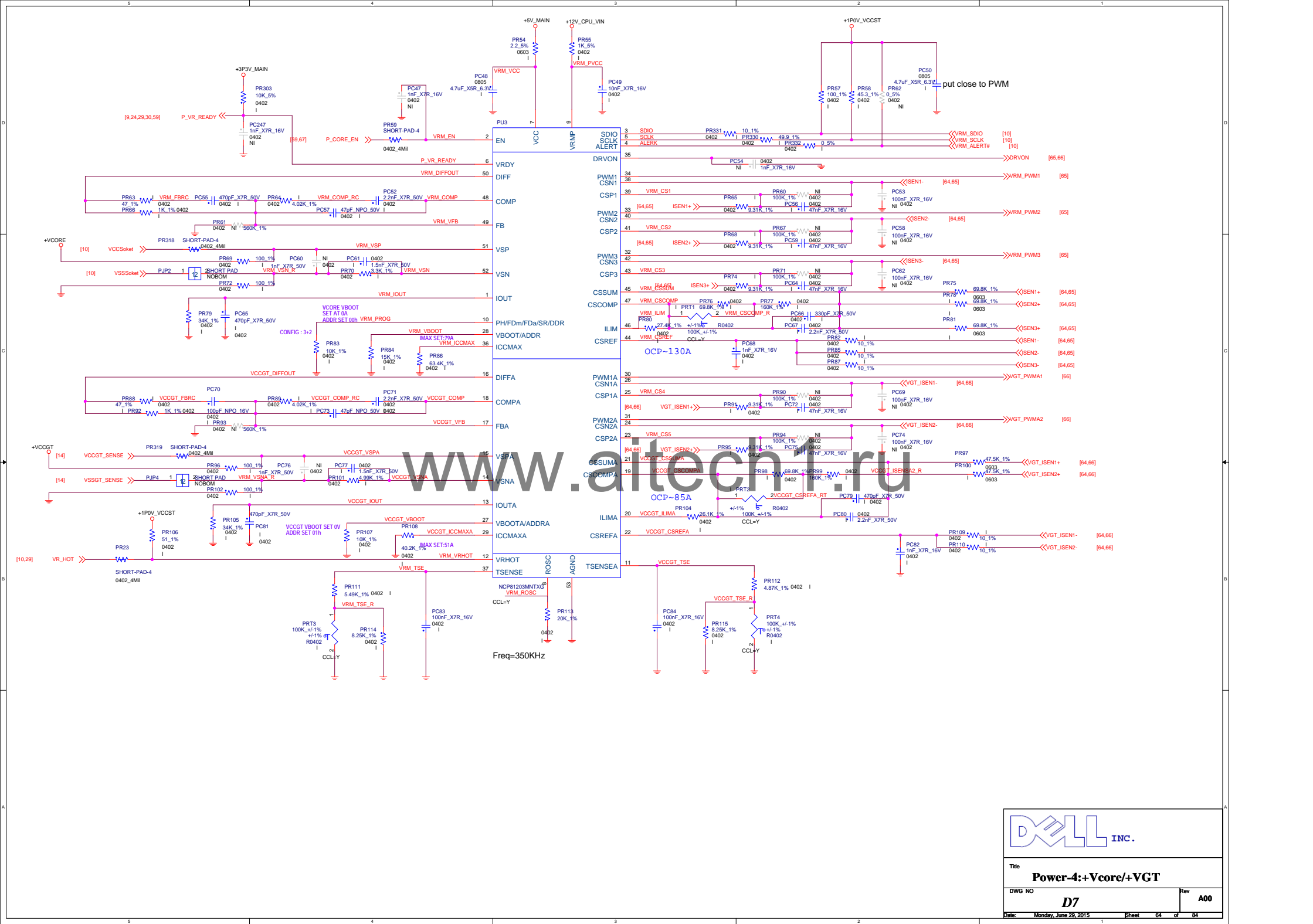


DELL INC.

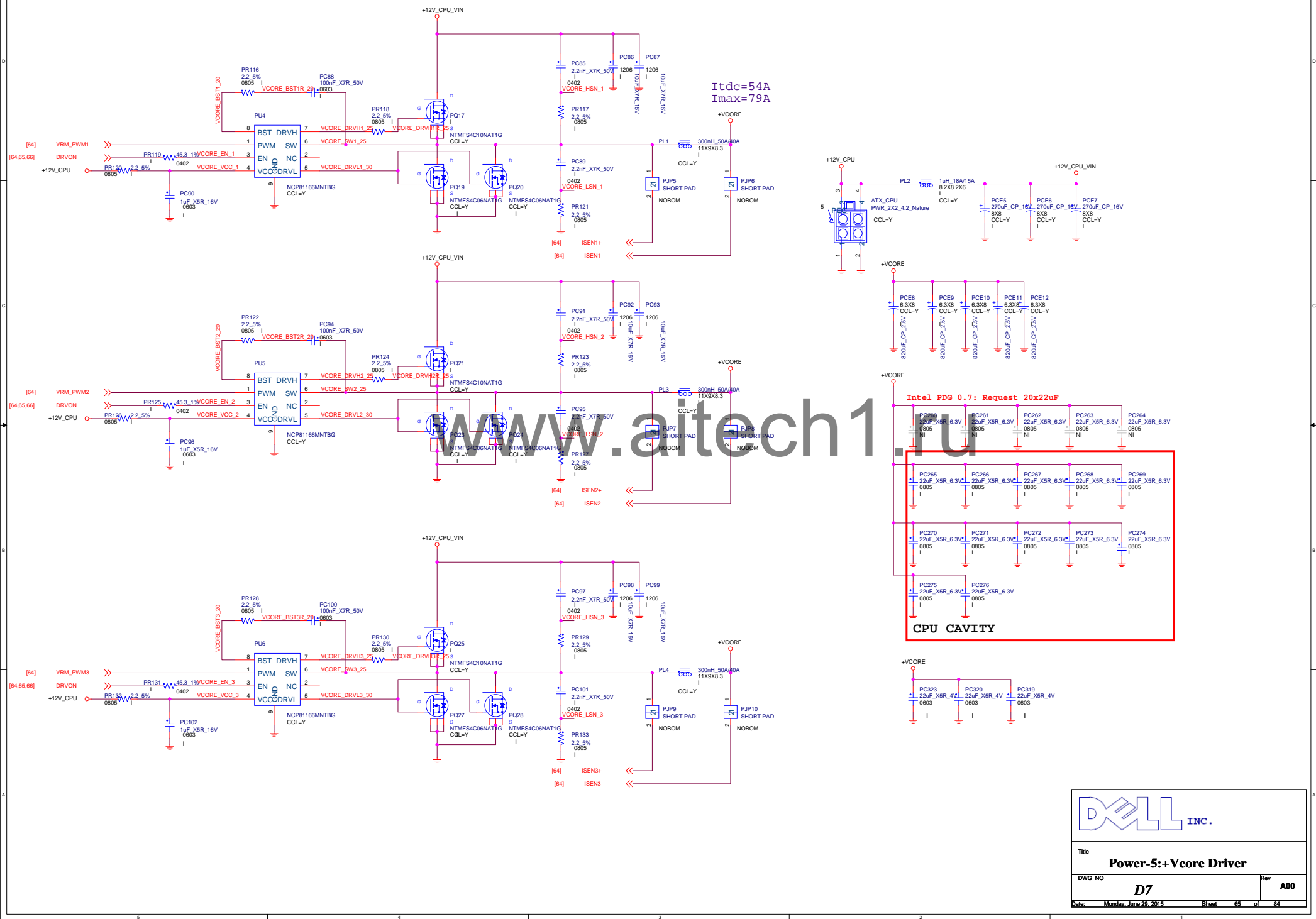
Title: **Power-2: Linear Power-2**

DWG NO: **D7** Rev: **A00**

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VCORE PHASE1~3

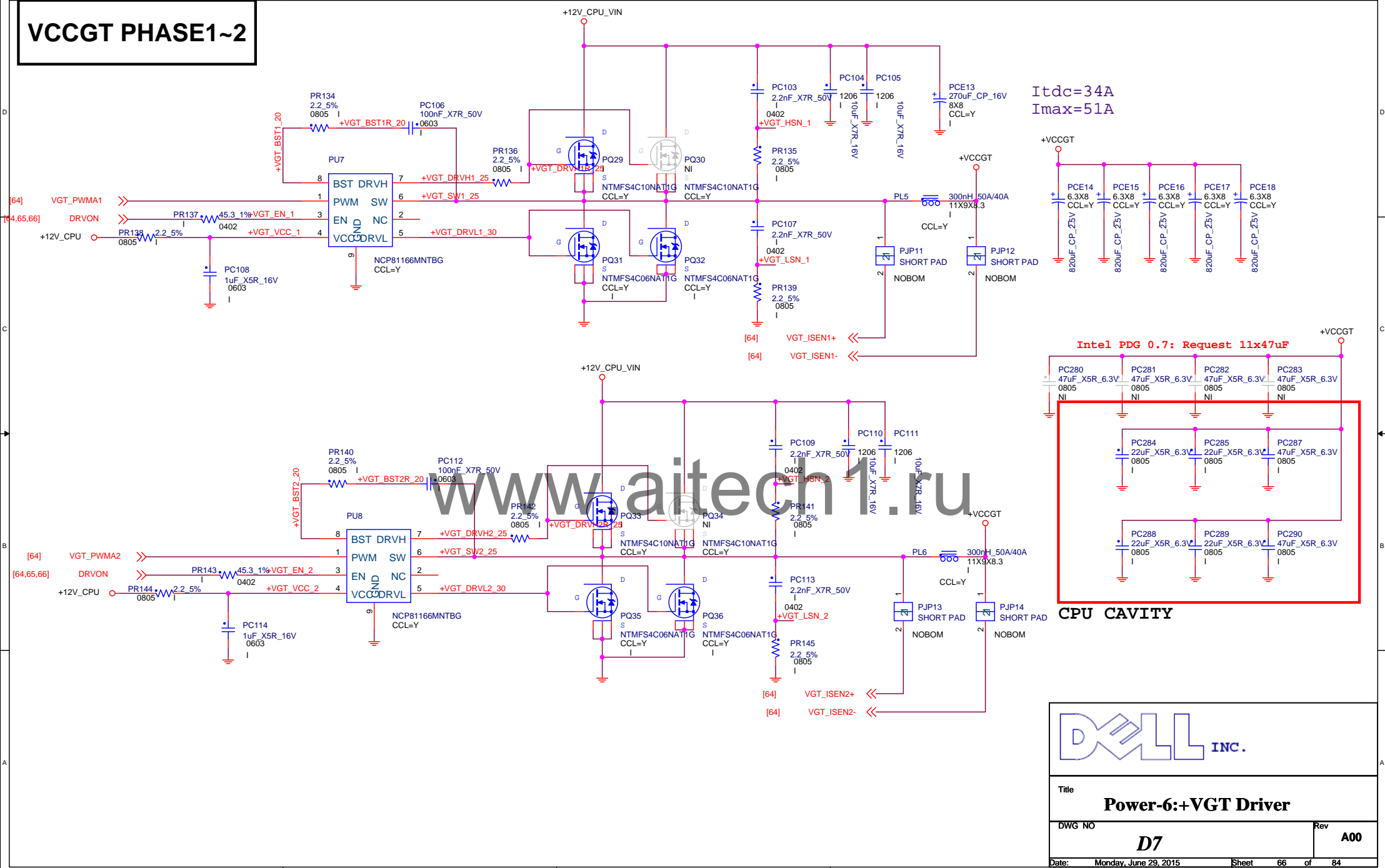


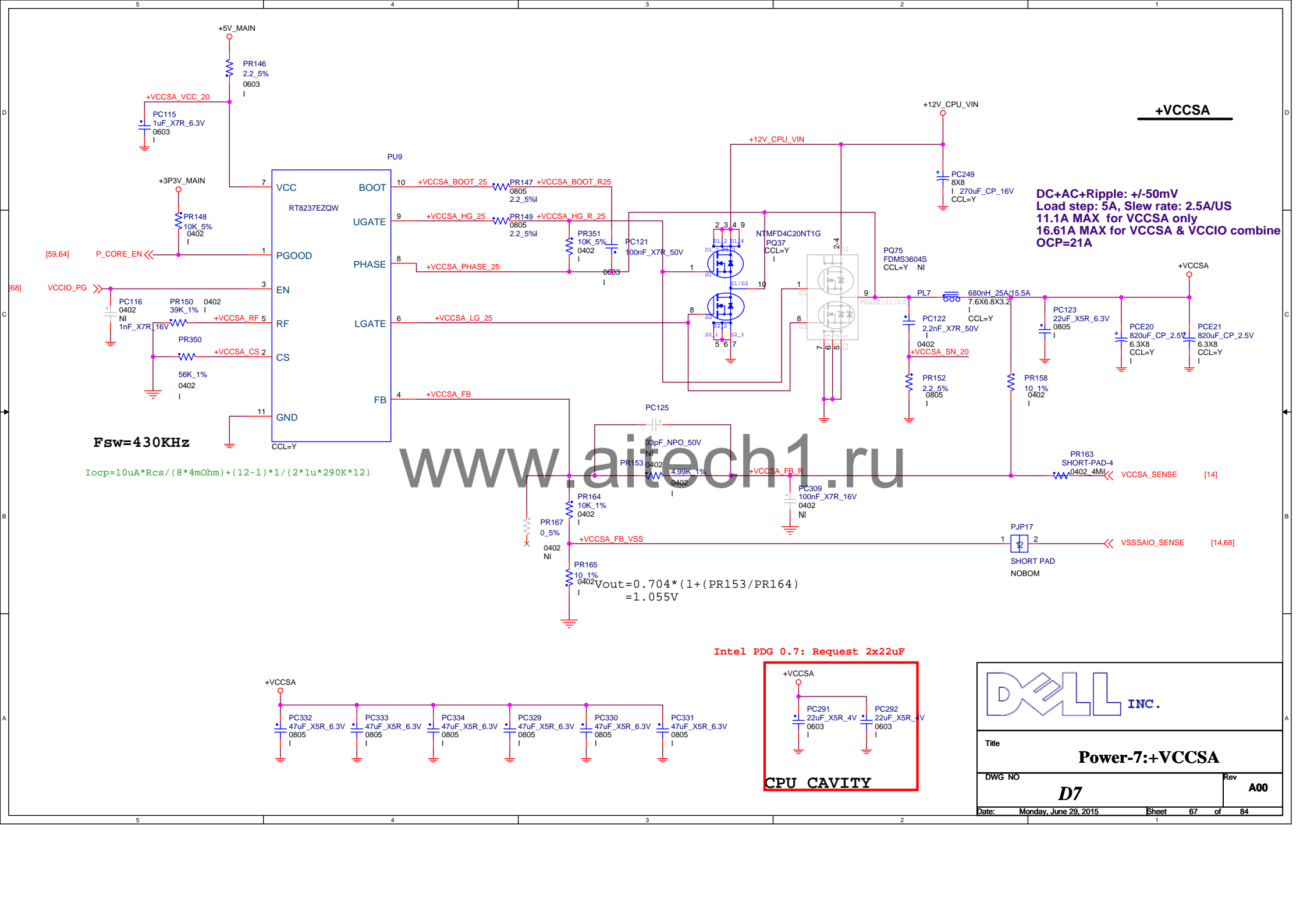
DELL INC.

Title **Power-5:+Vcore Driver**

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VCCGT PHASE1~2





+VCCSA

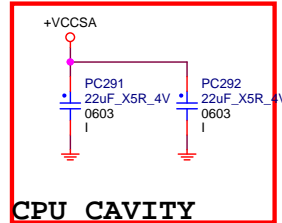
DC+AC+Ripple: +/-50mV
Load step: 5A, Slew rate: 2.5A/US
11.1A MAX for VCCSA only
16.61A MAX for VCCSA & VCCIO combine
OCP=21A

Fsw=430KHz

$$I_{ocp} = 10\mu A * R_{cs} / (8 * 4m\Omega) + (12 - 1) * 1 / (2 * 1\mu * 290K * 12)$$

$$V_{out} = 0.704 * (1 + (PR153 / PR164)) = 1.055V$$

Intel PDG 0.7: Request 2x22uF

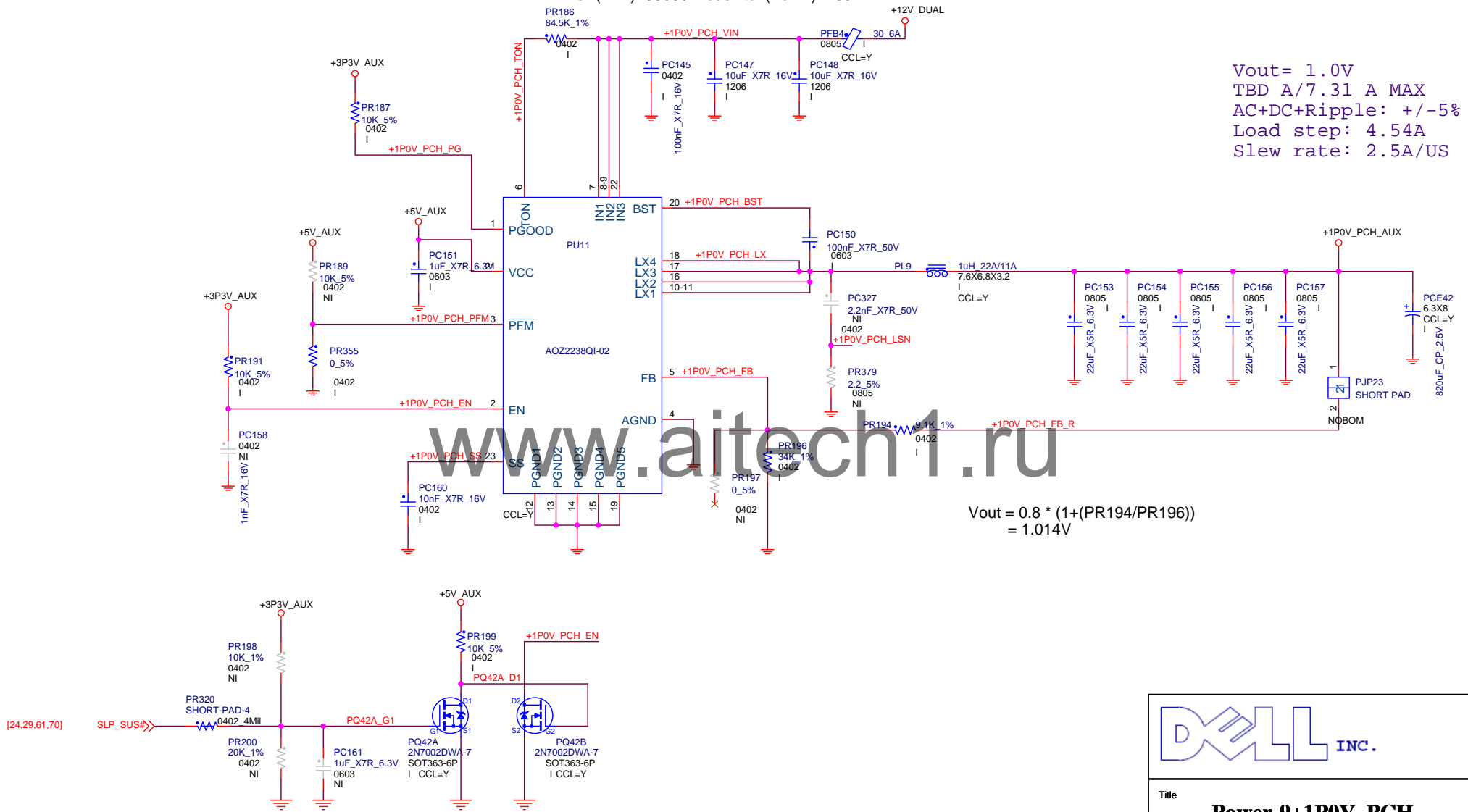


DELL INC.		
Power-7: +VCCSA		
DWG NO	D7	Rev A00
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+1P0V_PCH_AUX

$$F_{sw}(KHz)=38000 \cdot V_{out}/R_{ton}(Kohm)=450KHz$$

$V_{out} = 1.0V$
 TBD A/7.31 A MAX
 AC+DC+Ripple: +/-5%
 Load step: 4.54A
 Slew rate: 2.5A/US



Title	
Power-9+1P0V_PCH	
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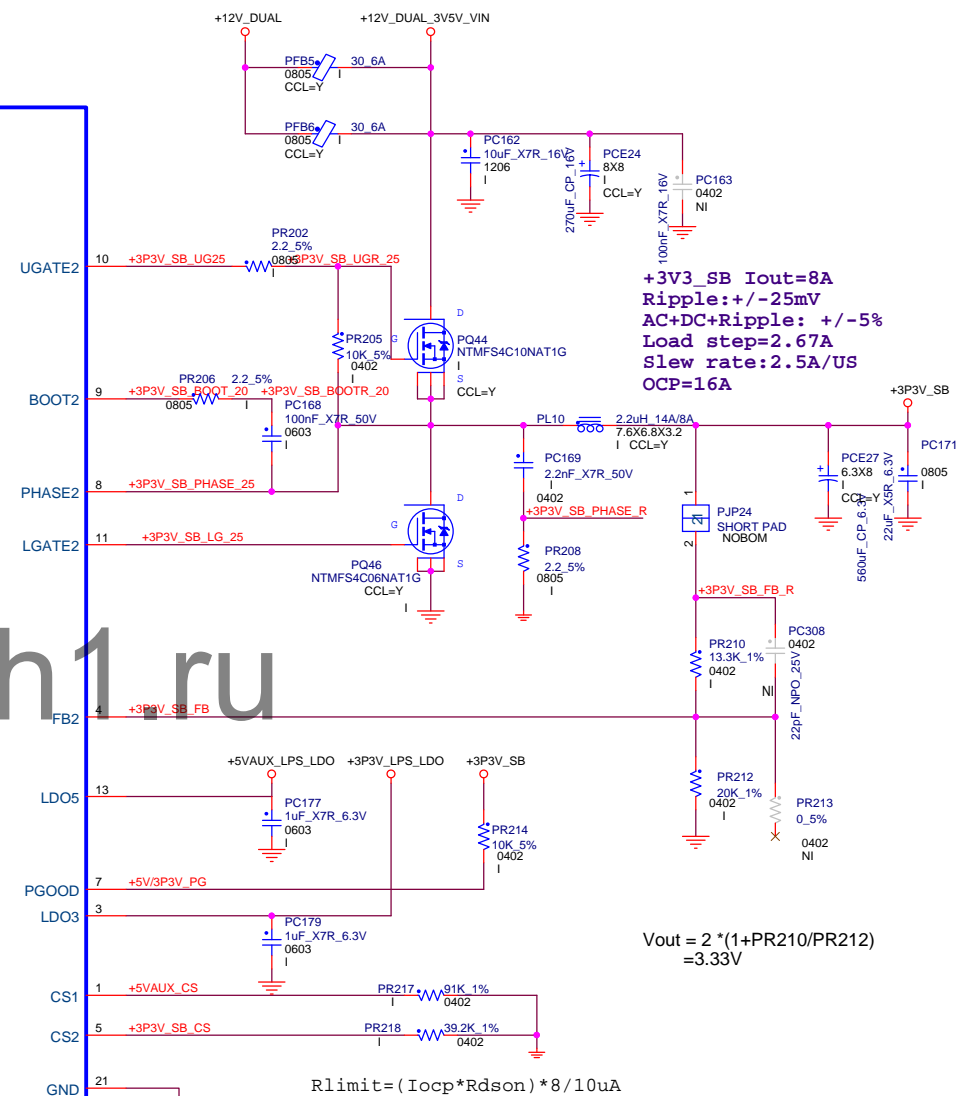
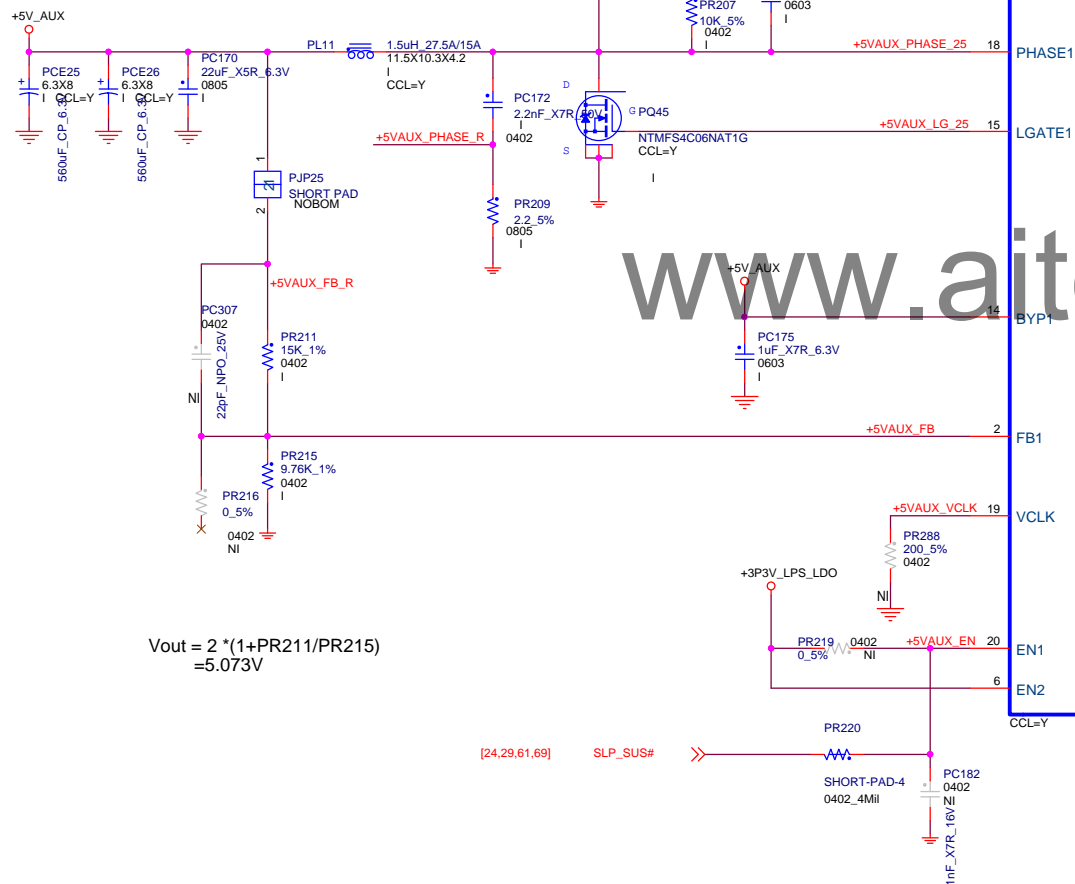
D


C

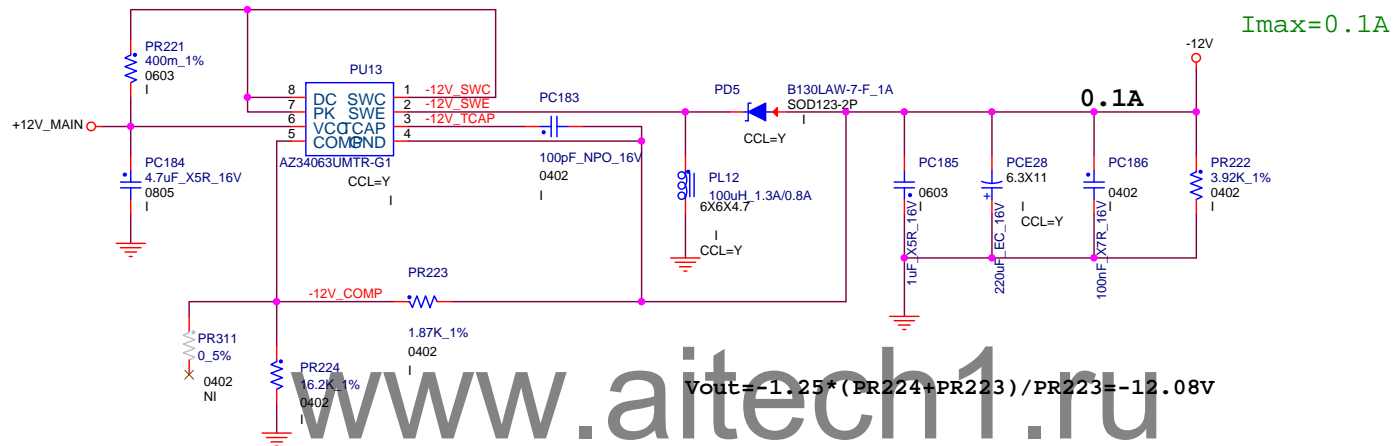
B

A

+5V_AUX Iout=15 A
 Ripple: +/-35mV
 AC+DC+Ripple: +/-5%
 Load step=5A
 Slew rate:2.5A/US
 OCP=30A



	
Title	
Power-10:+3P3V_SB/+5V_AUX	
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Title			Power-11:-12V	
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Title

TBD

DWG NO

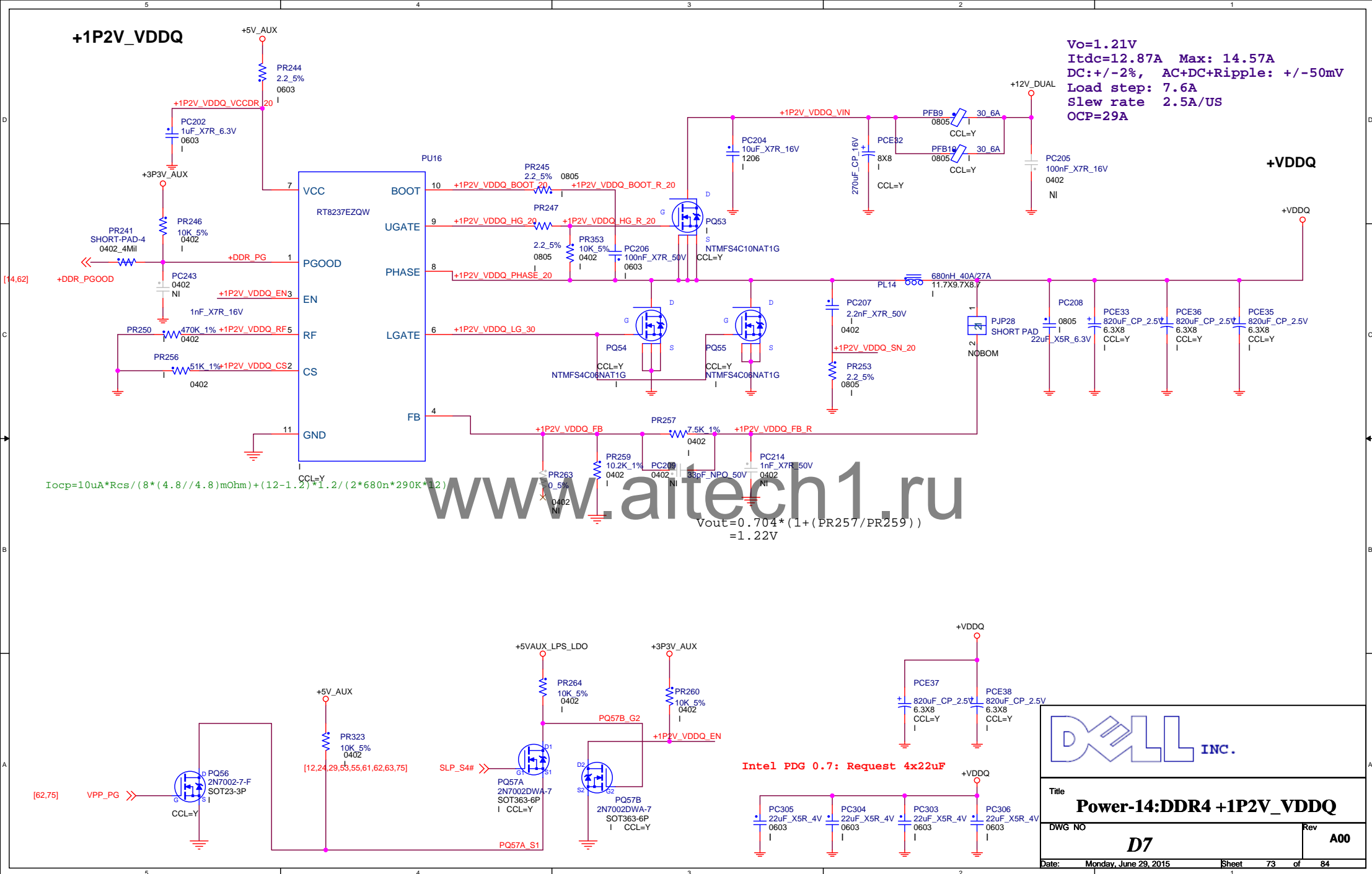
D7

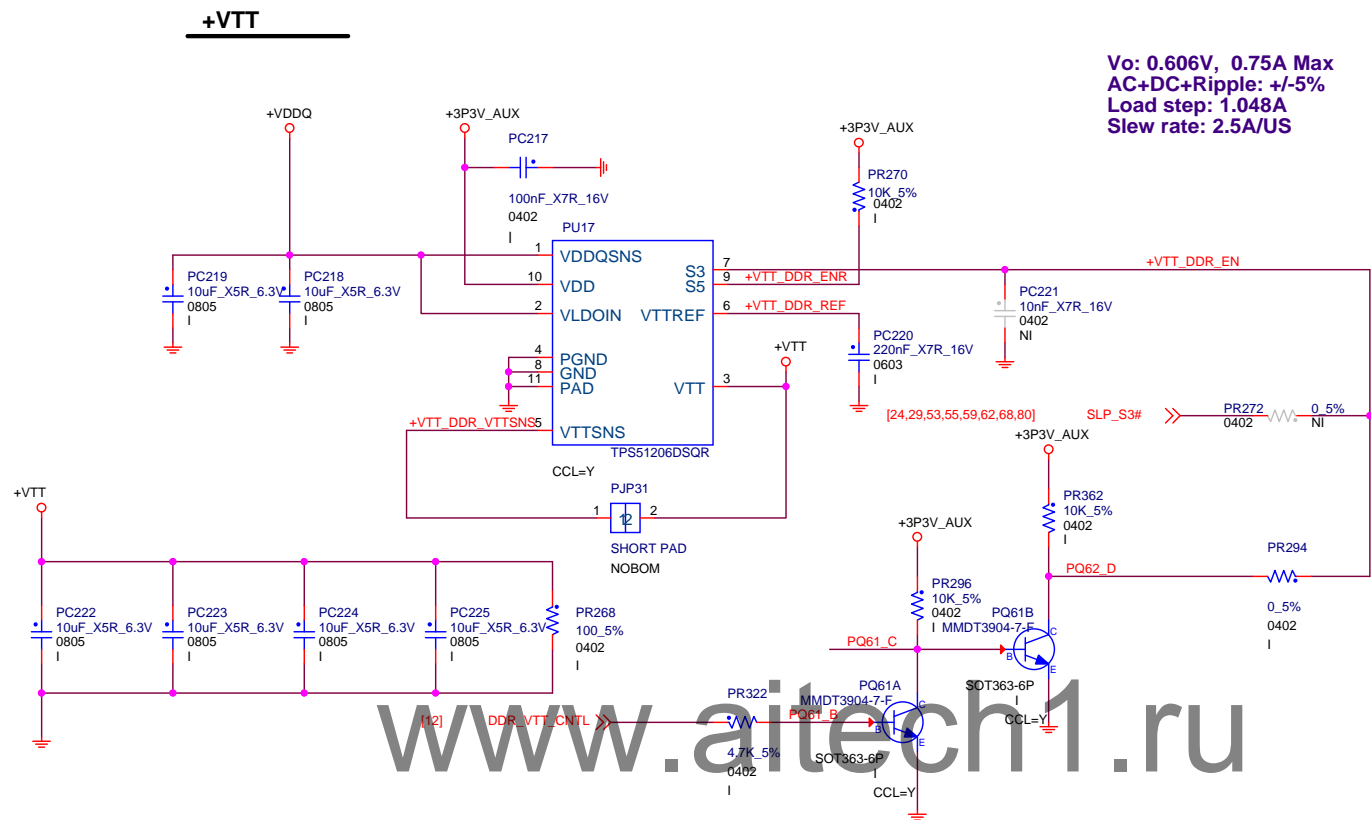
Rev

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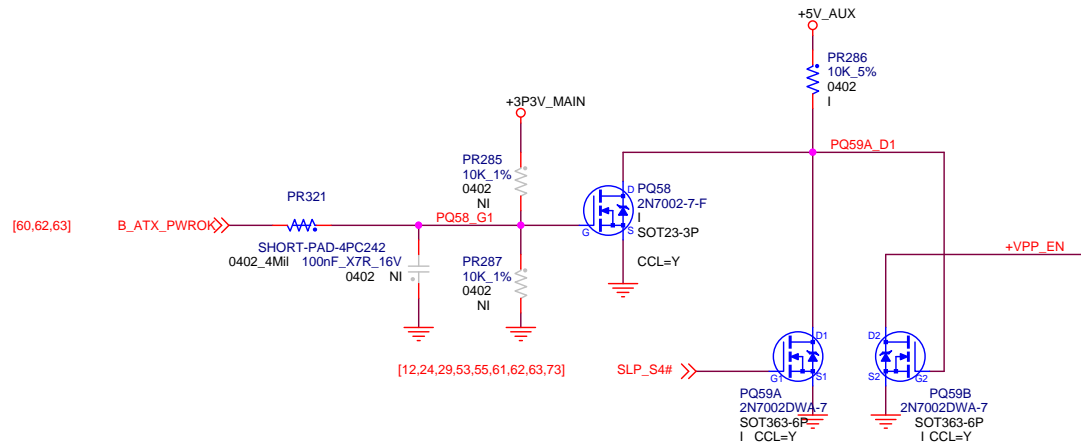
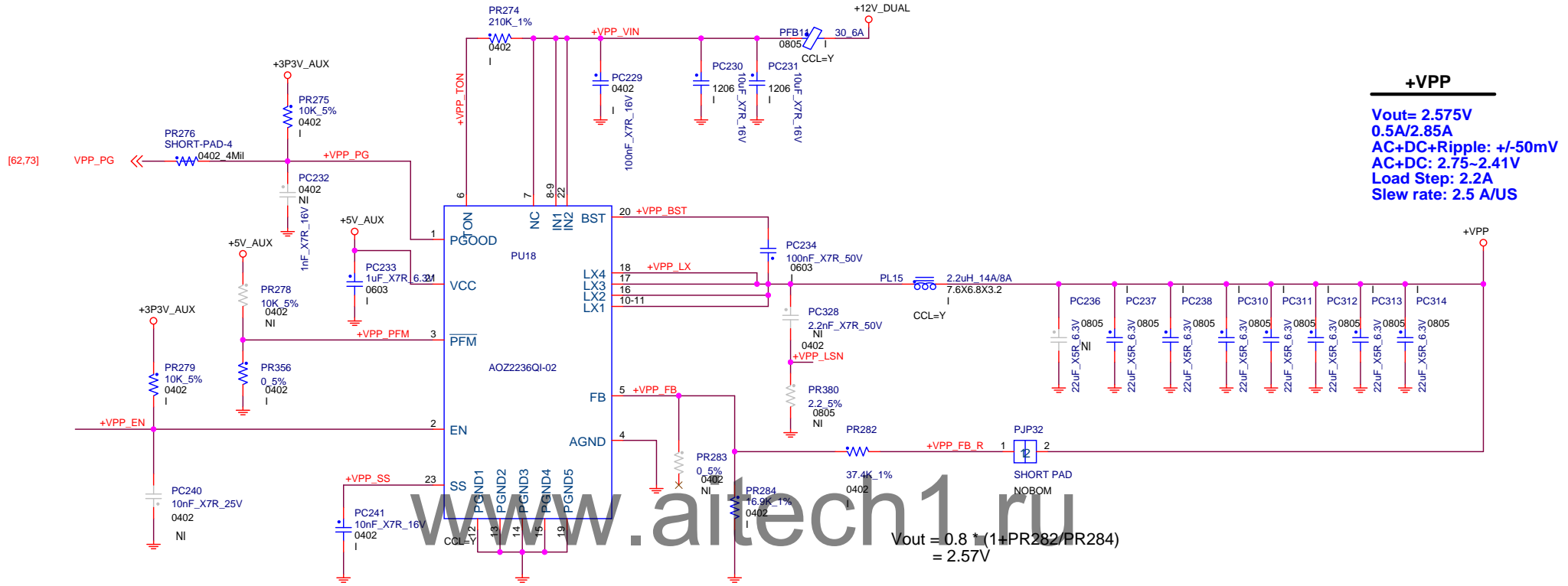




Title Power-15:DDR4 +VTT_DDR	
DWG NO D7	Rev A00
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+VPP

$$F_{sw}(KHz) = 38000 * V_{out} / R_{ton}(Kohm) = 450KHz$$




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Title		Power-16:DDR4 +VPP	
DWG NO	D7	Rev	A00
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Intel PCH XDP Debug Connector

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Project	
Spitfire	V
Scorpion	V
Toledo	V

 INC.	
Title	
CPU	
DWG NO	Rev
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Intel PCH XDP Debug Connector

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Project	
Spitfire	V
Scorpion	V
Toledo	V

 INC.	
Title	
CPU	
DWG NO	Rev
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Intel PCH XDP Debug Connector

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Project	
Spitfire	V
Scorpion	V
Toledo	V

 INC.	
Title	
CPU	
DWG NO	Rev
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Intel PCH XDP Debug Connector

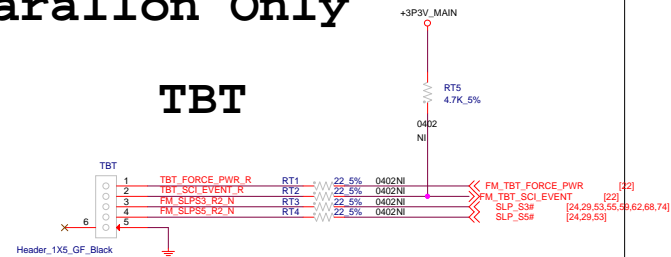
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Project	
Spitfire	V
Scorpion	V
Toledo	V

 INC.	
Title	
CPU	
DWG NO	Rev
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Farallon Only

TBT




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Intel PCH XDP Debug Connector

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Project	
Spitfire	V
Scorpion	V
Toledo	V

 INC.	
Title	
CPU	
DWG NO	Rev
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Intel PCH XDP Debug Connector

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Project	
Spitfire	V
Scorpion	V
Toledo	V



Title

CPU

DWG NO

D7

Rev

A00


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Intel PCH XDP Debug Connector

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Project	
Spitfire	V
Scorpion	V
Toledo	V

 INC.	
Title	
CPU	
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